NASA Contractor Report 172554

# Feasibility of Self-Structured Current Accessed Bubble Devices in Spacecraft Recording Systems

G.L. Nelson, D.R. Krahn, et al.
Advanced Materials and Devices CTC
SPERRY Corporation
P.O. Box 64525
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Contract NAS1-16911
April 1985



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# PREFACE

The following persons participated in some way in the technical work described in this report:

| | |
|---|---|
| R. H. Dean | G. L. Nelson |
| M. A. Fisher | M. C. Paul |
| D. R. Krahn | C. H. Tolman |
| D. S. Lo | E. J. Torok |
| C. J. Nelson | C. T. Burilla |

Project engineer for the first two years of this project was C. H. Tolman. The completion of this project was directed by G. L. Nelson.

Portions of this report were written by R. H. Dean, D. R. Krahn, G. L. Nelson and M. C. Paul. Appendix B was written by D. S. Lo and Appendix C was written by D. L. Amundsen and G. A. Stein.

This report describes work done by the Sperry Corporation under NASA Contract NAS1-16911. The initial NASA program director was Dr. R. Stermer, Jr. Mr. P. J. Hayes continues in that role.

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SECTION

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## 1.0 Introduction: Scope, Outline and Summary of Important Results

This report covers the device component, architecture, and comparative technology survey results obtained on Self-Structured Bubble Memory development under NASA contract #NAS1-16911. In addition, where noted, the report briefly covers related data coding results from Sperry IR&D funding. This work was performed in the period from March 1982 to February 1985.

The goal of the self-structured bubble memory approach is to make significant improvements in speed, density, and cost compared to conventional bubble memory devices. The results described in this report indicate that data rates from 1.5 - 10 megahertz in a 10 megabit chip with no need for redundant storage loops, areas, or associated control electronics are potentially feasible while obtaining good fabrication yields. As a result, the authors believe that further effort to develop this technology is warranted.

The overall format of the report is such that major tasks in the device development efforts are covered in the main sections of the report. Appendices cover some detailed fabrication results, the Memory Component Survey, and the Memory System Study. A brief description of the most significant sections follows.

Section 2 covers the preliminary device architecture and component ideas used as a basis for experimental component-test-chip design, build, and test efforts. A component in this report refers to a building block element of a memory chip design, an example is an I/O track. This section also covers the data coding results obtained to date on the complementary Sperry funded effort.

Section 3 describes the experimental component-test-chips design, build, and test results. The most significant results of this work were the demonstrations of garnet saturation-mobility limited data rates, the successful propagation of bubbles in a circuit with deliberate lithography defects, and the demonstration of the major components needed for a complete memory chip. These results formed a basis for device architecture design efforts and power/thermal modeling covered in Section 4. Section 3 also covered the general fabrication techniques and the test electronics used in the experimental evaluations.

Section 4 covers two general approaches to a 10 megabit memory chip based on the self-structured approach and components experimentally developed. Two specific designs

for each approach are covered. The first approach satisfies the NASA goal of an 18 storage area device. The second approach describes an 8 storage area device designed on the complementary Sperry IR&D project. Detailed power modeling of the NASA design is presented to address overall chip power consumption and device thermal constraints.

Appendix B is a comparative survey of the different memory technologies including bubble and self-structured bubble.

Appendix C is a comparative study of several memory technologies from a system point of view and with a specific spacecraft application as a basis. The results indicate that projected self-structured bubble memory devices are very competitive in this representative application.

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## 2.0 Preliminary Device and Component Set Design

### 2.1 Introduction

This section of the final report presents overall memory device designs and component set elements which formed the basis for the subsequent experimental development described in Section 3. The designs presented provided a starting point for experimental development of a chip meeting the NASA requirements: self-structured, current access bubble memory device with 18 distinct regions (16 + 2 redundant) cumulatively holding $10^7$ bits on a 1.5 cm by 1.5 cm chip with shift rates greater than 1.5 megabit/sec.

The designs presented provide increased storage density, reduced lithography requirements, and better yield than extrapolating conventional bubble devices. These result from the self-structured and critical feature approaches used in the design and discussed below.

Self-Structured - the concept of self-structuring used in the following designs is to use either a mix of stripes and bubbles or simply an array of bubbles. The principal benefits are an increase in density of magnetic domains in the storage area, from conventional non-interfacing separations to much closer proximities with interaction, and a capability for surrounding domains to exert forces on a particular domain to hold it in place or to move it past a defect. The density improvement in going from an array of nominally non-interacting bubbles with separations approximately 5 times the bubbles diameter to a bubble lattice with spacings of 2.5 the bubbles diameter is a factor of 4. This significant increase in density is achieved without a change in bubble size or in the minimum lithography dimensions which in the worst case in a self-structured device will still approximate the bubble diameter. A data coding scheme which has bubbles in every storage cell is required in a self-structured device. Two approaches are being developed to satisfy this constant. One uses double magnetic layer (111) garnets, the other uses single layer (110) garnets. (See 2.3.10). The ability to move domains past defects will be discussed further in the critical feature paragraph below.

Critical feature - The device designs presented rely on a reduced number of critical features and decreased lithography resolution requirements for a given data density rather than, for example, eliminating lithography from the storage area. Critical features are defined as features in the lithography which if not perfect, will prevent proper device operation. Examples are shorts between permalloy elements or opens in conductors which upset control of a bubble, local area, or large region of a device. These preliminary designs reduce the number of critical features and increase device yield in three ways.

1) Eliminating permalloy elements from the storage regions, and thus eliminating the possibility of mishapen or residual permalloy features trapping bubbles or otherwise disrupting domain motion.

2) The replacement of propagation features with complex shapes or small minimum dimensions with simpler shapes, such as rounded holes or slots in the apertured current sheet approach. Also features designed so that the most common defects have a minimum effect on propagation behavior.

3) The close packed nature of a self-structured device making the domain motion tolerant of inoperative features, particularly with the elimination of permalloy features.

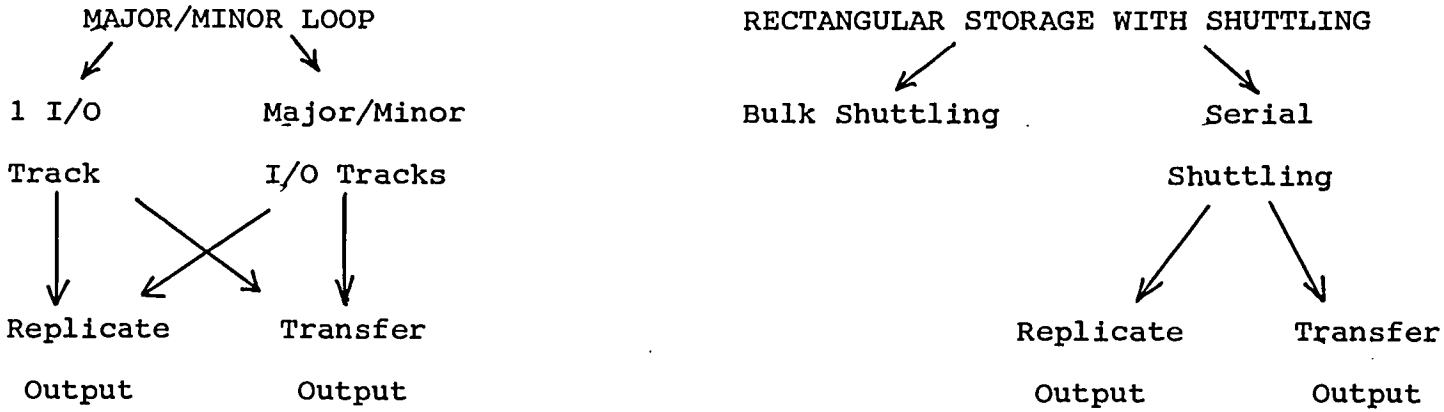
It is possible that this defect tolerant approach allows the elimination of redundant loops in the memory device while still achieving good fabrication yields. The benefits would include better use of die area in the memory chip and a considerable reduction in control requirements and silicon real estate. It has been estimated that up to 66% of the typical bubble memory control silicon area is required to handle the redundant loop overhead [1]. From a board level perspective, the smaller package size of a 10 bit current access memory chip (elimination of X & Y field coils) and a reduction in controller silicon would allow a significant advance in board level bubble memory performance.

## 2.2 Overview of Preliminary Device Designs

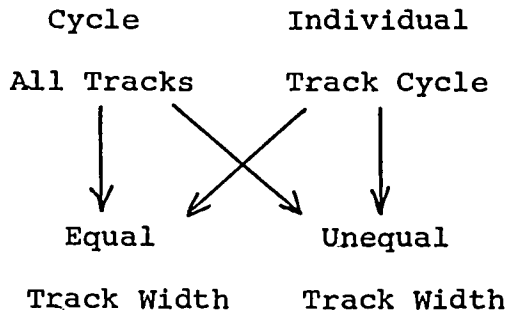
Based on past work sponsored by NASA and Sperry IR&D, it is believed that a derivative of apertured current sheet operation is the best device approach. Accordingly, the three preliminary designs presented here use this operating mode.

Three major device topologies and related components are described:
A) rectangular storage with shuttling,
B) concentric circular, and
C) major/minor loop
Of these, A and B reflect the direction at the beginning of the contract when lattice storage of stripes and bubbles together was planned. Approach C depends on being able to slip columns of bubbles past one another in a self-structured arrangement; something not known to be possible at that time.

With the successful demonstration of column slipping in a self-structured bubble arrangement, the C approach becomes the preferred approach. All of the experimental results and the device architecture designs in Sections 3 & 4 reflect this. As a result, the device component and architecture subsections relating to approaches A and B can be skipped if desired. They are included only for completeness and have an asterix before the subsections they number to identify them (subsections 2.2.2, 2.2.3, 2.3.2, and 2.3.6).




CONCENTRIC CIRCULAR




Three major device topologies and variations have been considered for the self-structured bubble memory device.

Table 2.2.1

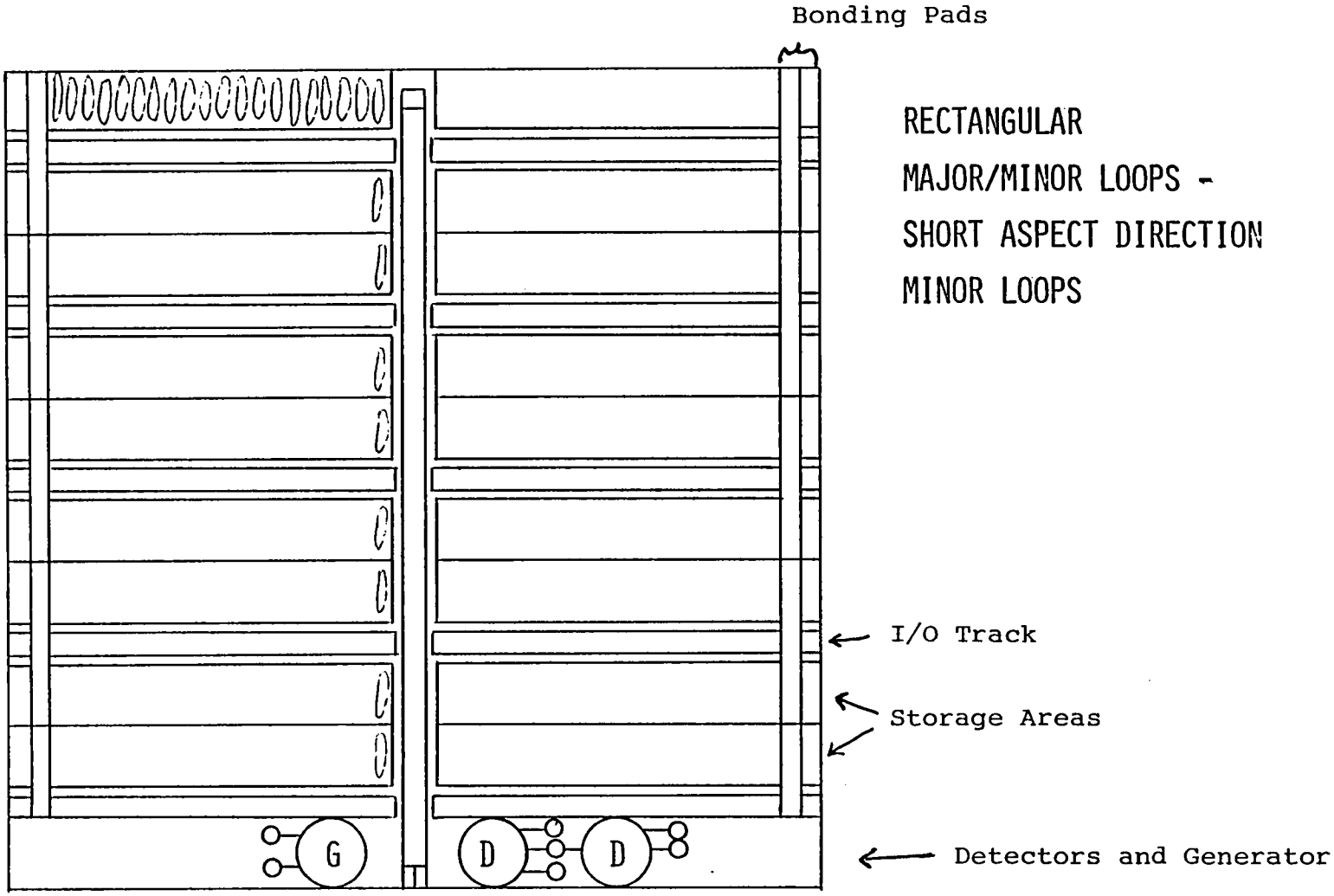
### 2.2.1 Rectangular Array with Major/Minor Loop Configuration

The first design to be discussed is a major/minor loop derivative with rectangular storage areas. A possible version is shown in Figure 2.2.1. In this design, two apertured conductors and a return ground plane over each of the 18 storage areas are used to rotate loops of bubbles in a direction perpendicular to the current flow directions. Transfer or replicate gates along the long dimension of each storage area pass data to minor I/O loops. Data is then passed along to the major I/O loop and detector. Writing would reverse the movement. Access to data located in the center of a storage area is rapid due to the short loops. Average power requirements are low due to both the 18 storage areas being separately drivable and the greater than 2K bits being read out/in each shift of the loops. The design minimizes package pin count and bipolar driver requirements by multiplexing driver pins with switchable ground planes. The result is 18 straightforwardly equivalent storage areas, individually driven, with good flexibility of operating modes with approximately 23 package pins depending on gating used to move bubbles in and out of the storage areas. The aspect ratios of the various elements in the design provide relatively high impedances for reasonable drive voltages and currents. A large percentage of the chip area is devoted to bubble storage area. An aperture arrangement with bubble spacing of 2.5 diameters, and assuming 90% of the device can be used as storage area, give a resulting bubble diameter of 1.8μ. A final practical note is that bonding pads occur at the periphery of the device.

### *2.2.2 Rectangular Storage Areas with Shuttling

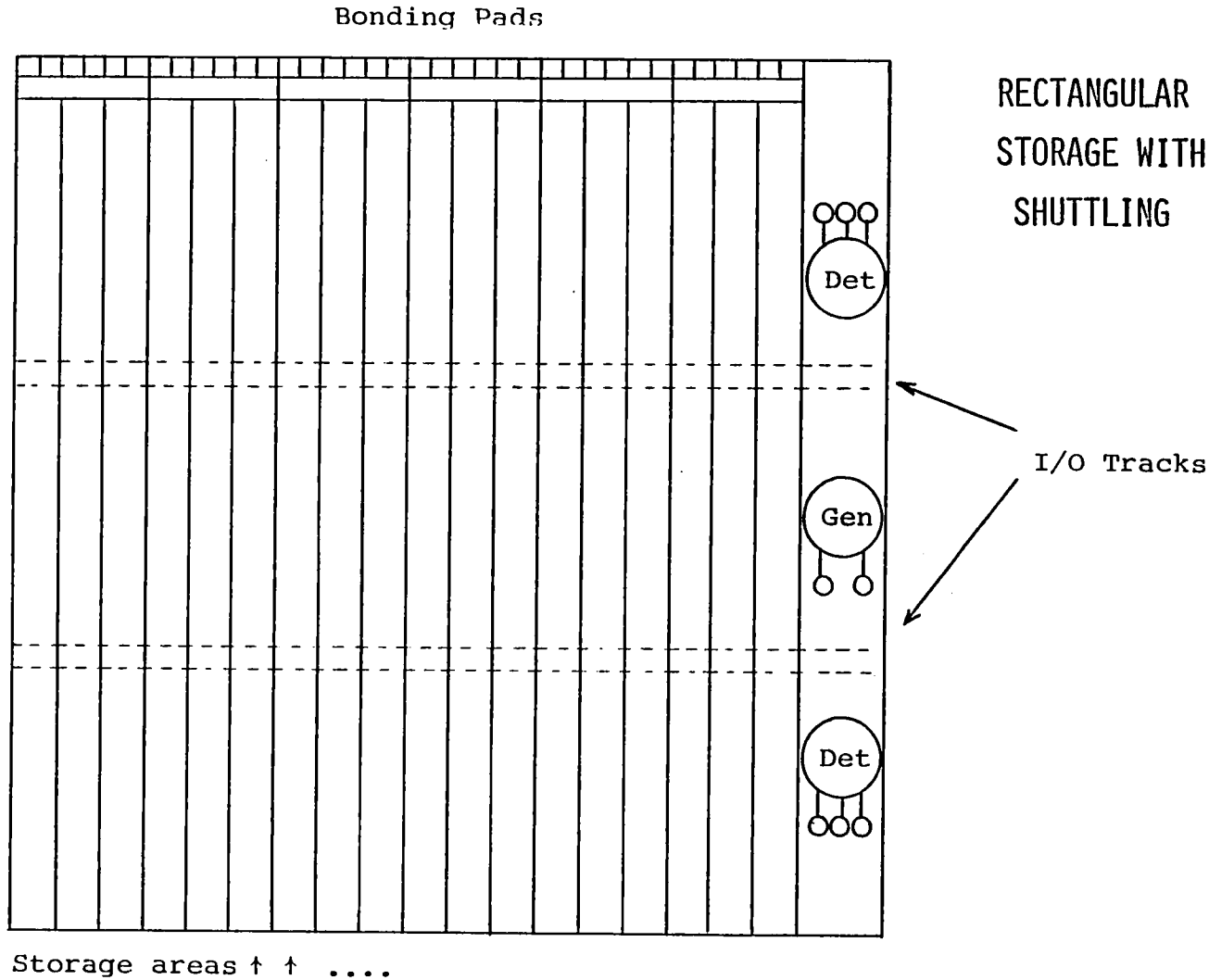
Another way to store data is to use an array which is shuttled back and forth over one or more I/O tracks. Figure 2.2.2 shows one possible configuration for implementing this approach. With two I/O tracks as shown, the effective storage area is only 2/3 of the actual storage area. However, since the bubble lattice can be compressed the maximum amount relative to the three general designs presented, and maintains straightforward geometry without needing stripes to keep bubbles organized around corners or slipping columns of bubbles, this area inefficiency is not totally uncompensated. The number of I/O tracks can be adjusted to make area efficiency and bubble size acceptable. A more serious shortcoming, however, is the need to keep the 'non-data' regions in each storage area filled with carrier bubbles to prevent the 'data' portion of the lattice from expanding. This required carrier bubble generation and annihilation at the ends of each storage area.

A more promising variation would be to strip a row of data out one end of the lattice before shifting and then feed the row back in at the other end. During the run from one end to the other, data desired as output could




Preliminary Bubble Memory Design

Figure 2.2.1




Preliminary Bubble Memory Design

Figure 2.2.2

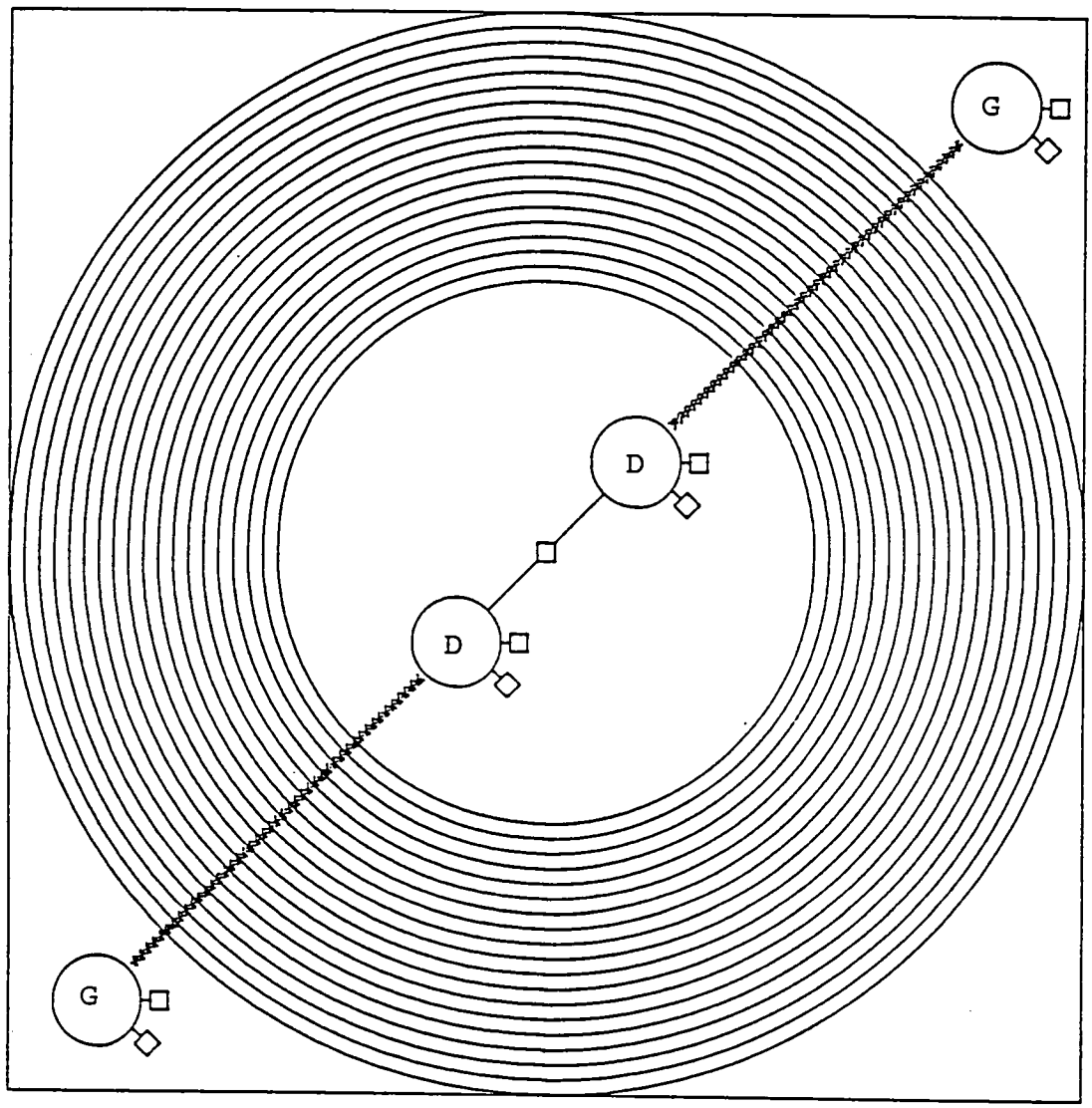
be replicated and sent to the detector. This approach would allow a maximum density lattice in rectangular storage areas with a high percentage of the chip devoted to storage. The major disadvantage would be access time determined by serial bubble rates rather than parallel rates. With a bi-directional shift track, operating at the I/O rate of 1.5MHz, maximum access time would be 185msec for an 18 storage region device. In a tape recorder equivalent application, this wouldn't matter, and in a more general memory application, a queing controller could take advantage of independent storage area control to frequently lower access time by shifting the next areas to be accessed while still reading out from the current area. Assuming 90% of chip area devoted to storage, no stripes required, and 2.5 bubble diameter lattice spacing, the required bubble diameter is 1.8 microns.

### *2.2.3 Concentric Circular Design

The concentric circular arrangement is shown in Figure 2.2.3. Referring to Table 2.2.1, there are two principal variables providing four general configurations. The two variables are cycling the 18 storage areas individually or together and using equal or unequal track widths. These will be discussed separately.

Cycling choice - shifting all storage areas together is a convenient choice of operation because it requires possibly only 3 package pins and 2 bipolar drivers for the propagation function. The I/O functions however, then require that data be read/written to all 16 areas simultaneously if anything near maximum data rates are required. If all data are being placed into one storage area, the I/O track must return the data temporarily removed from the other storage area I/O track regions before the storage areas can be advanced. This would be a severe limitation for a tape recorder type application needing high average data rates. Applications with smaller data batches which can tolerate access delays between bursts would operate well. Additional complications which need to be experimentally addressed are methods of slicing up the storage area to improve the voltage current drive needed. Generally, this will increase the number of conductor layers from 2 to 4. The other concern is the effects on margins of the nonuniform current densities.

Shifting storage areas individually increases the package pin count and need for pin multiplexing to equivalency with the other designs. However, being able to shift an individual area allows high data rates from each area rather than only the device as a whole. It also allows




Concentric Circular Tracks Configured With Either Radial or Individual Track Currents.

Preliminary Bubble Memory Design

Figure 2.2.3 .

more flexible control of the device. Drive voltage/current are somewhat compromised due to the very high average aspect ratio of the storage areas and varying aspect ratios of different storage areas. Making electrical connections to the storage tracks in this approach is also a challenging practical problem.

Track Width - Assuming that an equal amount of data will be stored in each of the 18 areas, the changing track length can be compensated either by spreading the data apart in the longer outer storage areas, or by decreasing the track width in the outer areas.

Maintaining equal track width and spreading the data circumferentially has the control advantage of an equal number of bits in the I/O track from each storage area (or an equal number moved into the I/O track shifting any area), and an equal number of shifts/360° rotation of data in any area. The disadvantages of equal track width are the constraint on amount of chip area occupied by storage area (39.9%) plus the inefficient use of area in outer tracks. In addition, the increased cell size in the outer tracks, as a minimum, will require stripe domains to maintain data order and worst case may preclude self-structuring.

The advantages of a variable track width include an ability to use more of the chip area for storage area, and all data being stored in a lattice of equal (maximum) packing density. The disadvantages fall in the control area in that different amounts of data are moved with each shift in the different storage areas, and different numbers of shifts/360° rotation are required for the different storage areas. This approach also accentuates the tendency towards high aspect ratio in the outer tracks and the variation in drive voltages required.

Summary - The circular track approach will probably require stripe domains along with the bubbles to keep data ordered moving around the track. This further reduces the effective storage area. Its advantages are that the circular arrangement does provide parallel lattice motion compared to the antiparallel slipping motion of the major/minor loop arrangement and without the moving lattice edge as in the rectangular shuttling approach.

## 2.3 Component Set Designs

For any of these device approaches to be experimentally achieved, a variety of components which form the building blocks for the various architectures must be possible. The following sections describe the approaches of interest in implementing these various components. The components covered are: propagation, barriers, I/O tracks, generation, gating, detection, and data coding.

### 2.3.1 Bubble Propagation

Bubble propagation by dual layer apertured current sheets has been demonstrated by a number of investigators including us [2]. There are two classifications of apertured sheet bubble propagators: those that propagate bubbles parallel to the current direction and those that propagate bubbles penpendicular to the current direction. These two types of bubble propagation are generally required for propagation in storage areas and I/O tracks. Both use four current pulses to propagate the bubble one unit cell distance. The four pulse sequence cycles through the two possible current polarities in each of the two conductors (see Figure 3.8.8).

Figure 2.3.1 shows two apertured current sheet designs for propagating bubbles parallel to the current direction. The design of (a) is preferable to (b) because the distance between apertures in the same conductor is larger. Also, the propagation margins on (b) should be much worse because of the necessity of trying to move the bubble from an equilibrium position in sheet 'one' to another equilibrium position in sheet 'one' by changing the pulse polarity. The bubble could go the wrong way unless a coincident pulse in sheet 2 is simultaneously applied.

Figure 2.3.2 shows an apertured current sheet design for moving bubbles perpendicular to the current. An advantage for this geometry is the presence of a repelling pole behind the bubble's position in addition to the attractive pole ahead when the next pulse in the propagation sequence is applied. This improves the efficiency of propagation.

These basic propagation approaches are used in subsections 2.3.2, 2.3.3, and 2.3.6 in lattice propagation, major loop propagation, and lattice storage I/O tracks respectively.

### *2.3.2 Array Propagate Structures

The two types of propagation, parallel or perpendicular to the current direction, can be used in structures which propagate bubble or bubble/stripe arrays. Perpendicular appears more promising; however both are considered.

Figure 2.3.3 shows an example of a perpendicular bubble/stripe array propagation structure. The array is a half lattice with one stripe per row of bubbles. The current is perpendicular to the bubble motion.

The complete propagation structure has a second apertured conductor sheet not shown that fits on top of the illustrated sheet. This second sheet is identical to that of Figure 2.3.3, but is spaced just half an aperture to the right.

The main purpose of the stripes is not to push the bubbles as in the design of the previous contract (NASI-15007), but to prevent the bubbles from becoming disordered. Just how many rows

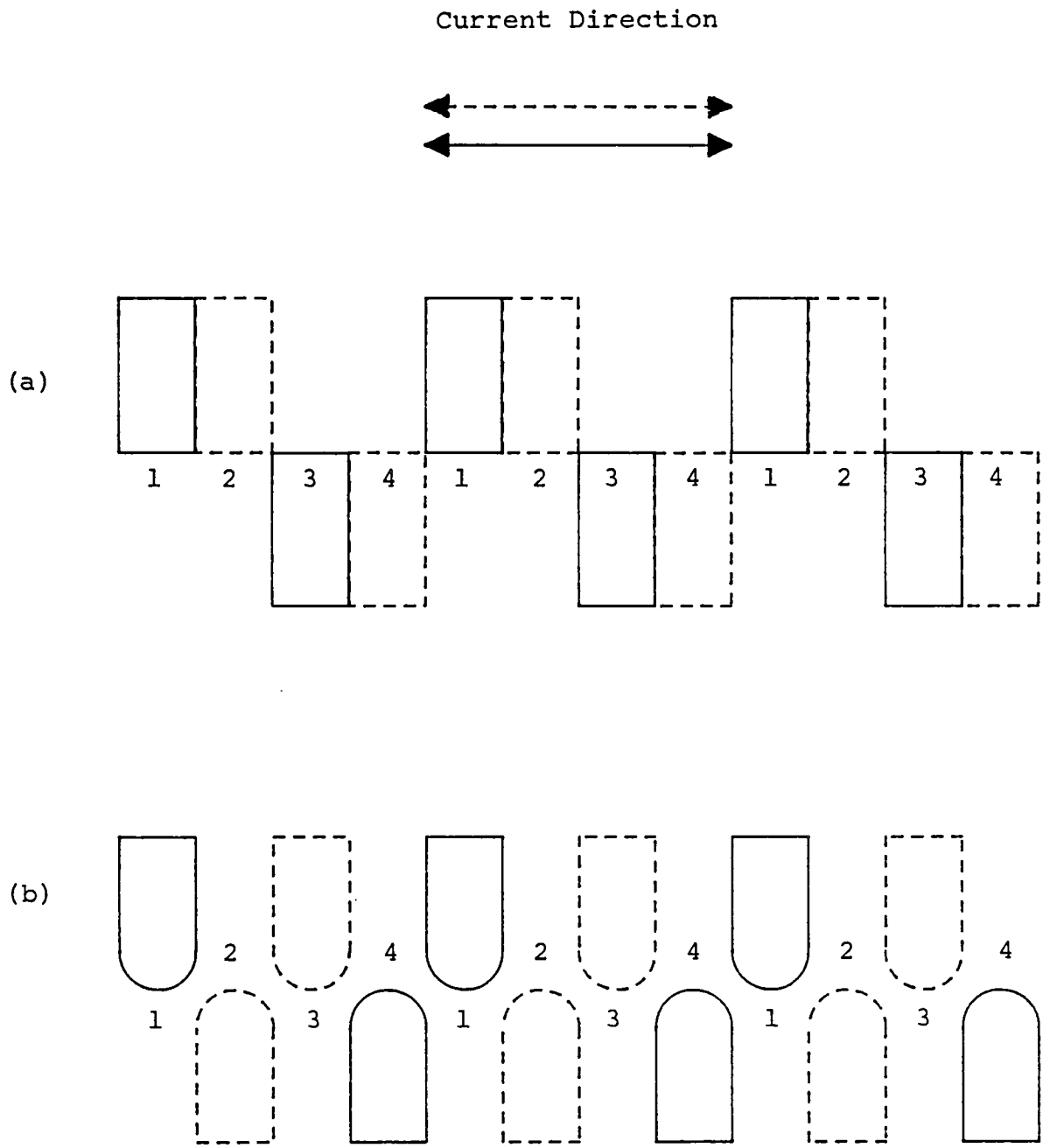



Figure 2.3.1 Two designs for propagating bubbles parallel to the current direction.

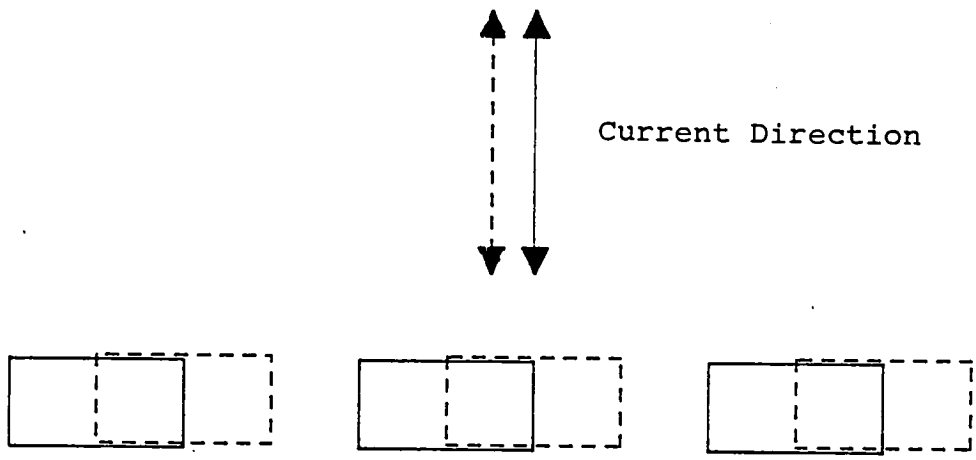



Figure 2.3.2 An apertured current sheet design that propagates bubbles perpendicular to the current direction.

of bubbles per stripe one can have without risking disorder is not known. It is important to determine the answer to this question, however, because the density of the memory depends greatly on it. It may be that the lattice is so stiff that no stripes are needed at all. Accordingly the designs of Figures 2.3.4 and 2.3.5 are of interest. If disordering can occur, the configuration of Figure 2.3.5 should reveal it.

Actually, any of the apertured sheet designs of Figures 2.3.3-2.3.5 will propagate any of the bubble-stripe configurations of any of the others. However, initialization of a particular stripe-bubble pattern can be achieved only with an apertured sheet that resembles the desired stripe-bubble pattern. Initialization is achieved by a single large pulse that nucleates stripes or bubbles below each aperture.

The configuration of Figure 2.3.6 shows an example of the second category of apertured current sheets: one in which the current flows parallel to the direction of propagation. The problem with this configuration is that stripes cannot be nucleated during the initialization pulse and, if stripes are required, they must be inserted from the side as data is inserted.

### 2.3.3 Major/minor Loop Storage Propagation

Another arrangement of the apertures results in a loop arrangement as shown in Figure 2.3.7 [ 2 ]. This structure has the bubbles propagating in both directions perpendicular to the current flow direction to make up the sides of the loop and parallel to the current flow direction at the ends of the loop. A structure made up of a group of these loops as shown in Figure 2.3.8 is of interest for the rectangular major/minor loop architecture. The important experimental question is whether the slipping of columns of bubbles past each other will function at the close bubble spacings of interest.

### 2.3.4 Ground Planes and Interconnect

It's desirable that the aspect ratio of a driven propagation area be such that it provides reasonably high load resistance. In the shuttle and major/minor structures, this is simply controlled using the aspect ratio of the rectangular storage area. For the circular structure, the radial current flow can be provided along with reasonable load characteristics either by wire bonding as shown in Figure 2.3.9 or by interconnections via a ground plane. The former should be quicker to fabricate

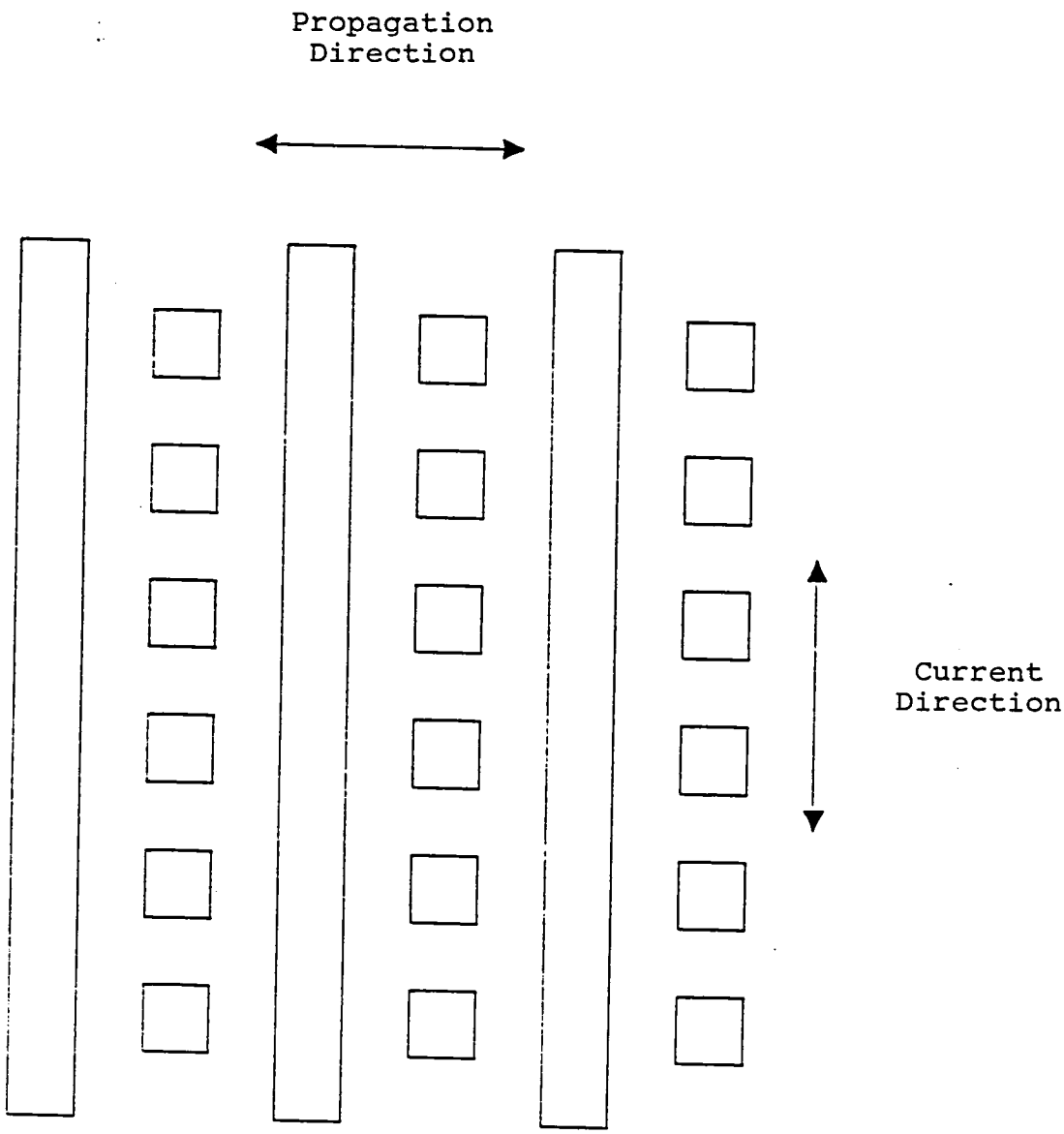
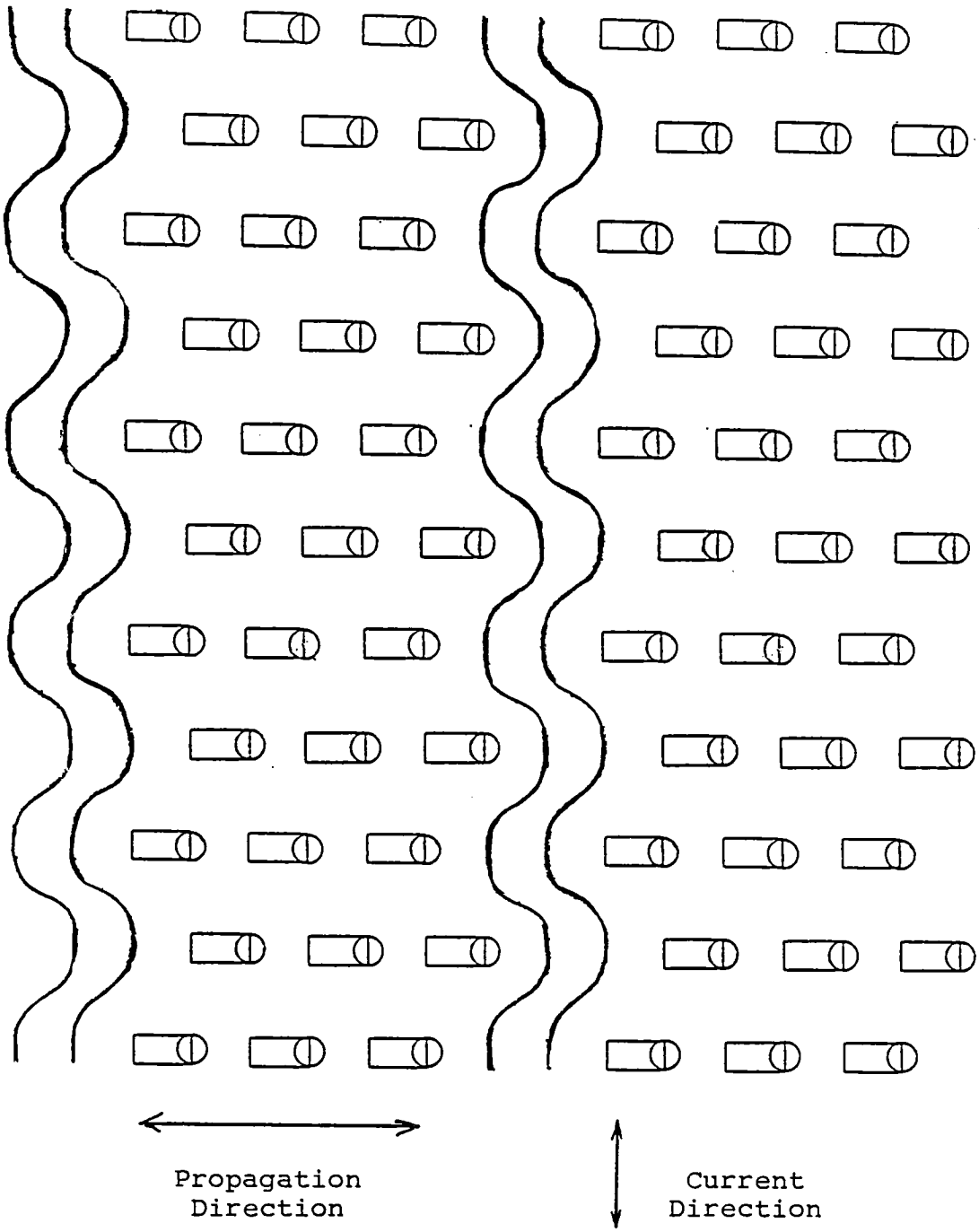



Figure 2.3.3 Half lattice array initiator and propagator




Propagation circuit with three rows of bubbles for every stripe.

Figure 2.3.4

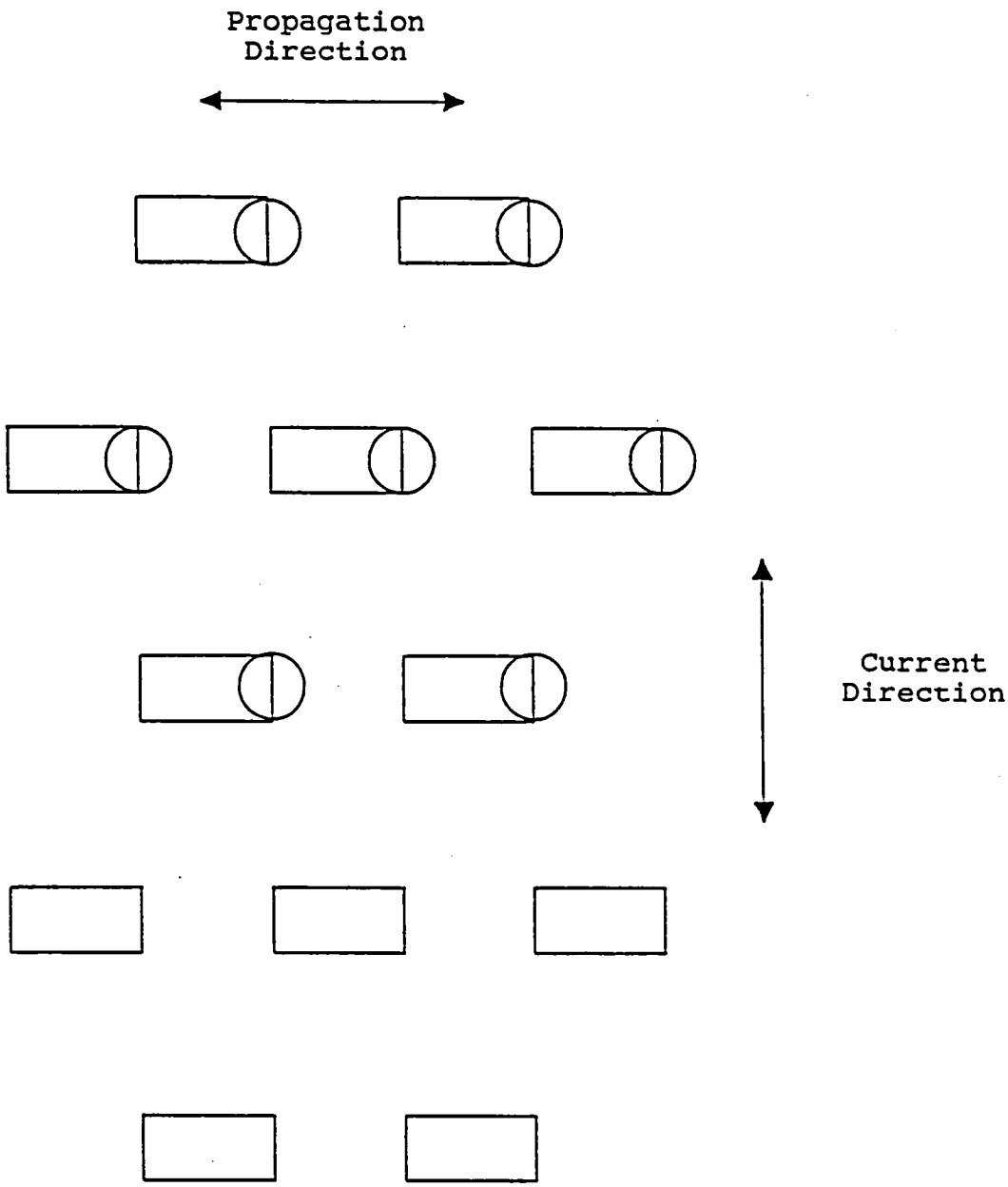
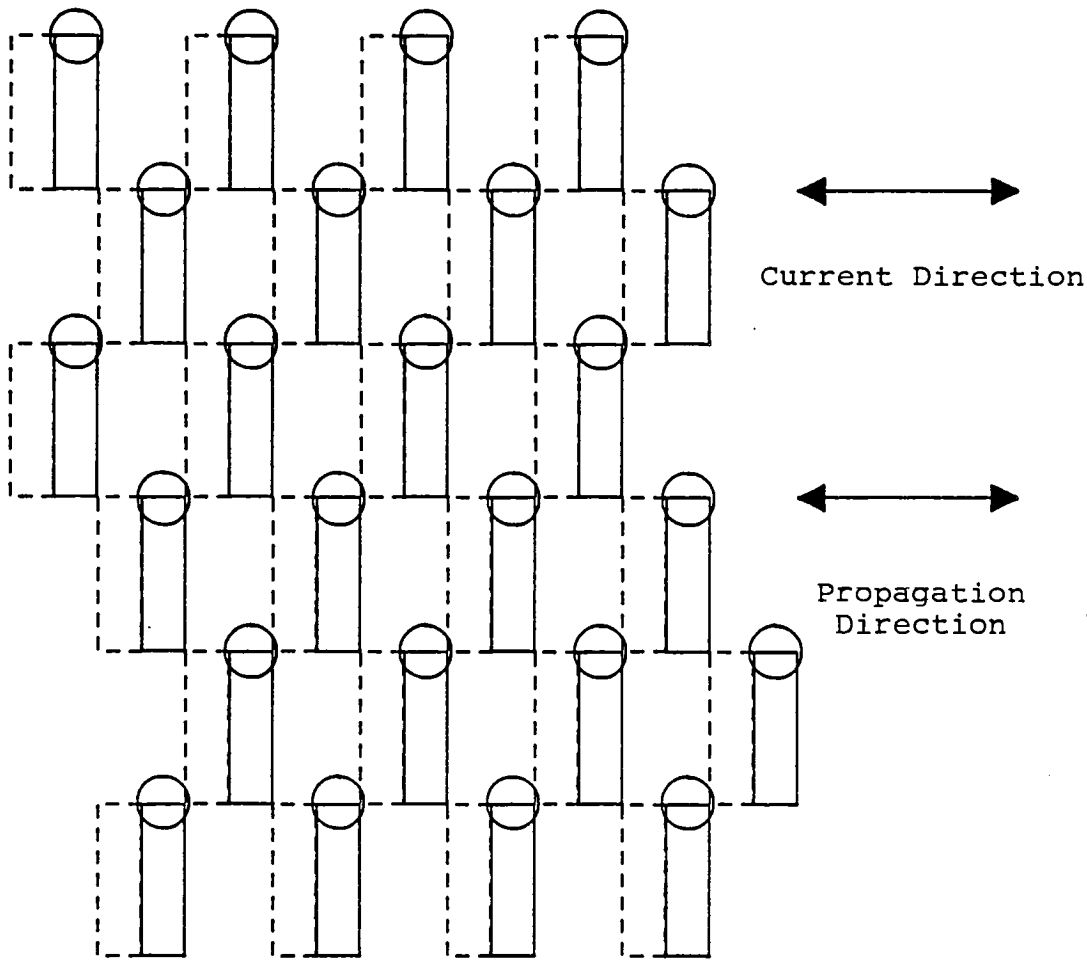
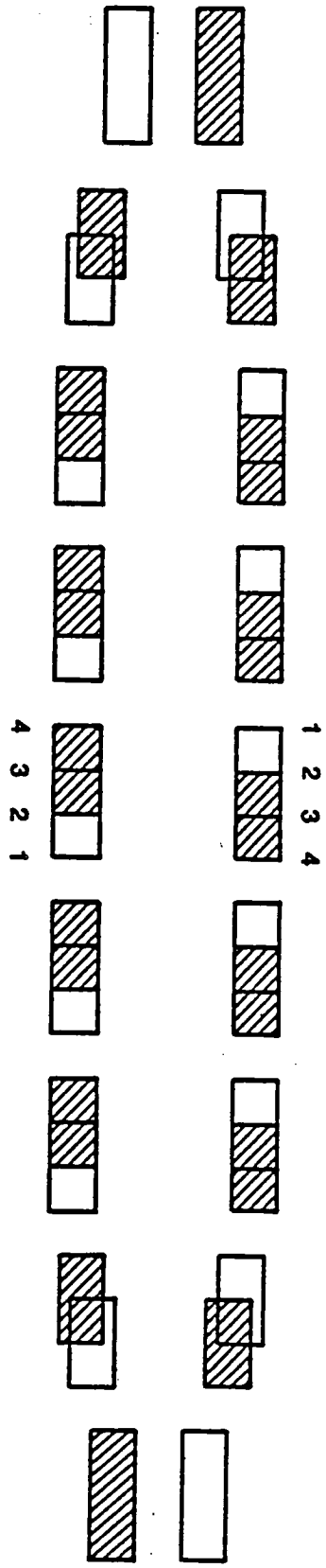



Figure 2.3.5 Configuration of apertures for initiation and propagation of a lattice with no stripes. Some bubbles are shown to indicate the hexagonal positioning.




Apertured current sheets that propagate a hexagonal lattice of bubbles parallel to the direction of current. The dashed lines represent apertures in the second current sheet.

Figure 2.3.6




Single Storage Loop for Propagating Bubbles Perpendicular to the Current Direction.

Figure 2.3.7

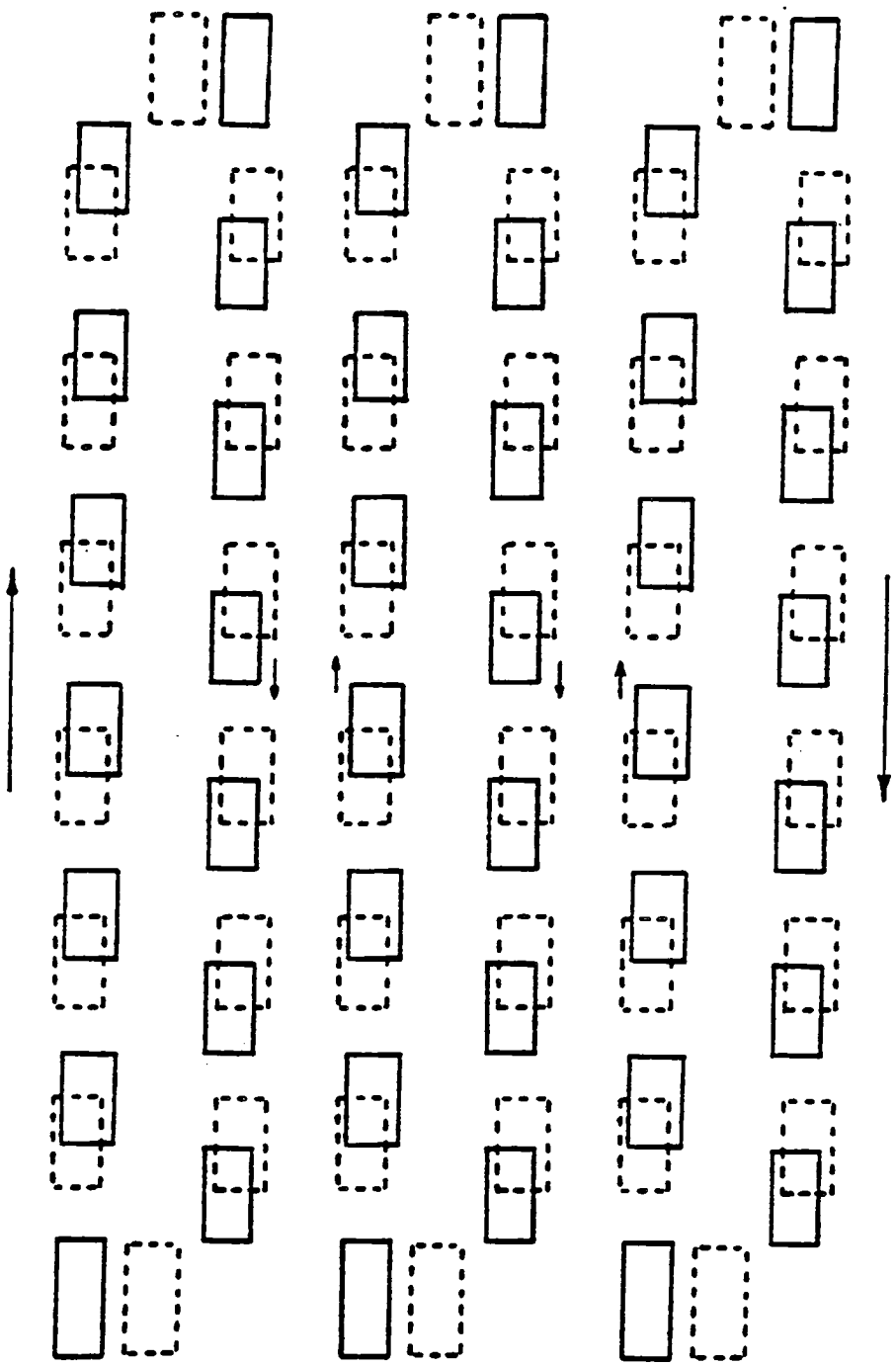


Figure 2.3.8 Triple loop for bubble lattice propagation in a column slipping mode.

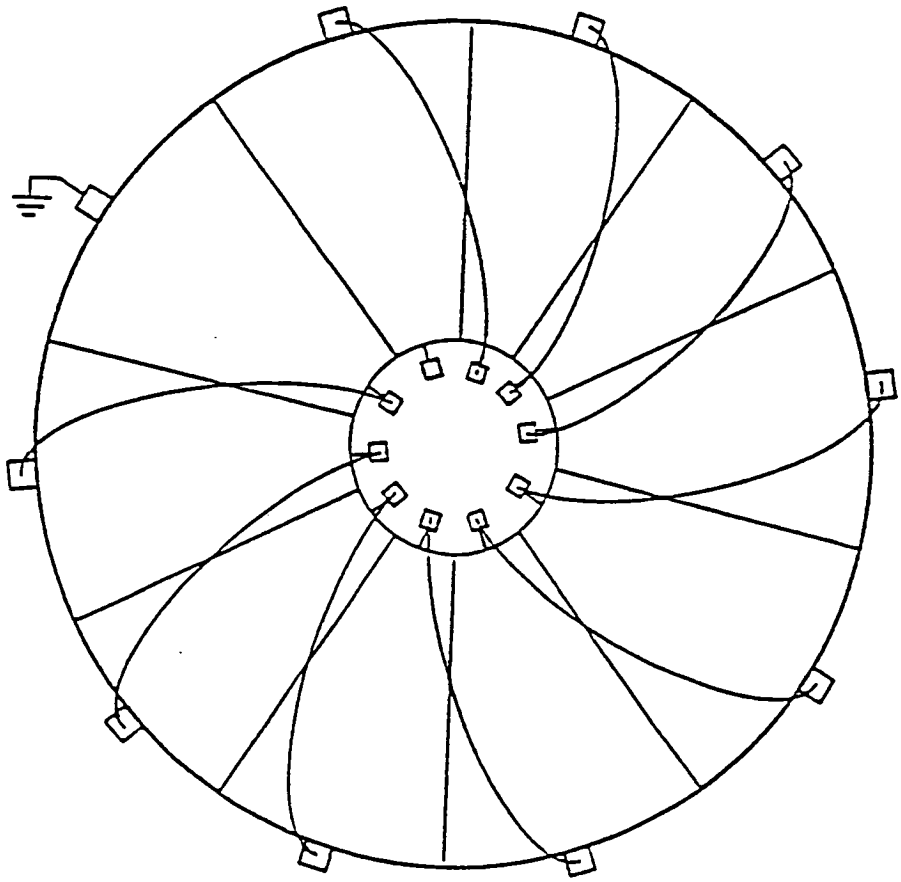


Figure 2.3.9 Current sheet chip divided into 10 sections, connected in series by wire bonding.

for experiments but the latter should be better for an operating memory, having more uniform fields and requiring nearly half the current and power if apertures are placed in the ground planes. Figure 2.3.10 shows part of an apertured current sheet to propagate bubbles and stripes around a circular track. Figure 2.3.11 shows the ground plane circuit that fits on top of it. The two layers are separated by a deposited insulating layer with vias for interconnection. The ground plane layer is placed on top but is displaced to the right by one aperture width. This is so that the fields from the apertures in both layers will add. Figure 2.3.12 shows how three such sections fit together. Current enters the apertured sheet from the lower left corner, travels through the apertured sheet to the via at the top of the page, enters the ground plane and exits at the lower right.

The full array propagation scheme requires two apertured current sheet ground plane pairs. This makes four conductor layers and two insulating layers total. In addition a keeper layer may be deposited on top. This strengthens the field from the circuits and thus lowers the required current by a factor approaching two and the power by a factor approaching four.

A three-layer device with a common ground plane is also of interest. This structure doesn't have apertures in the ground layer but is used to provide a cancelling edge field for the overall conductor. By eliminating the edge effect, a greater percentage of the propagation structure can be actively used. It is essential to eliminate the edge effects if propagation elements such as storage areas and I/O tracks are to be adjacent to each other.

### 2.3.5 Barriers

Because of the repulsive forces between domains in the self-structured device, barriers are necessary for containment and control at least at the edges of storage regions and possibly of I/O tracks. The most straightforward method appears to be ion milling to produce a step change in garnet thickness. Possible structures are milling around the storage area resulting in a mesa region, milling in the storage area resulting in a recess region, milling a channel around the storage area, or milling craters or simulated bubbles around the storage regions (Figure 2.3.13). An alternate approach for forming these structures would be to ion-implant at doses large enough to demagnetize the relevant garnet volume rather than physically removing it. This has the advantage of providing a planar surface for subsequent processing. Magnetostriction and thermal stability behavior, however, need to be accommodated.

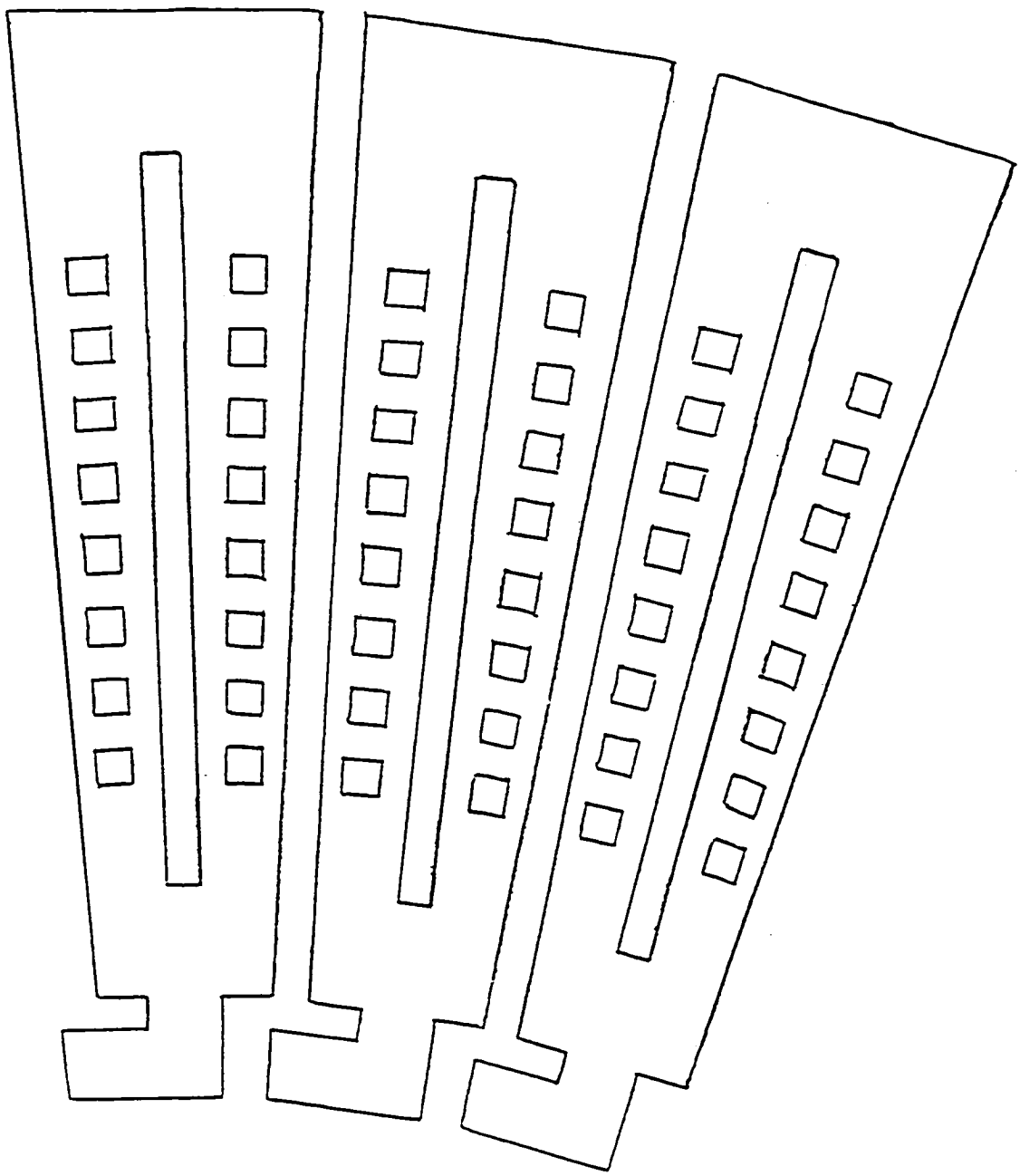


Figure 2.3.10 First conductor layer to be deposited for an array propagator around a circular track.

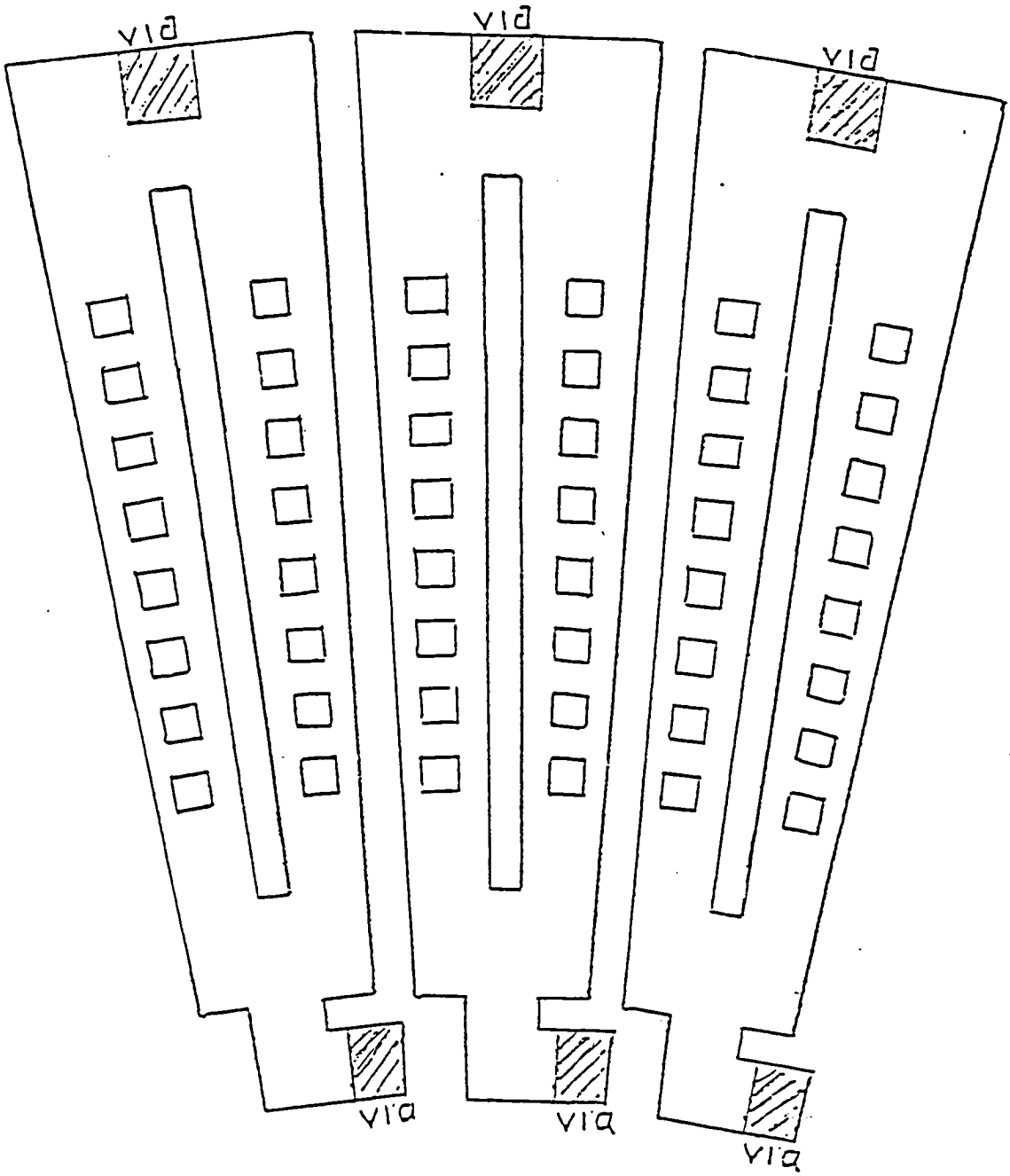



Figure 2.3.11 Second metal layer to be deposited for an array propagator. This is the so-called ground return circuit. This layer is separated from that of Fig. 2.3.10 by an insulating layer. The vias in the insulation are shown.

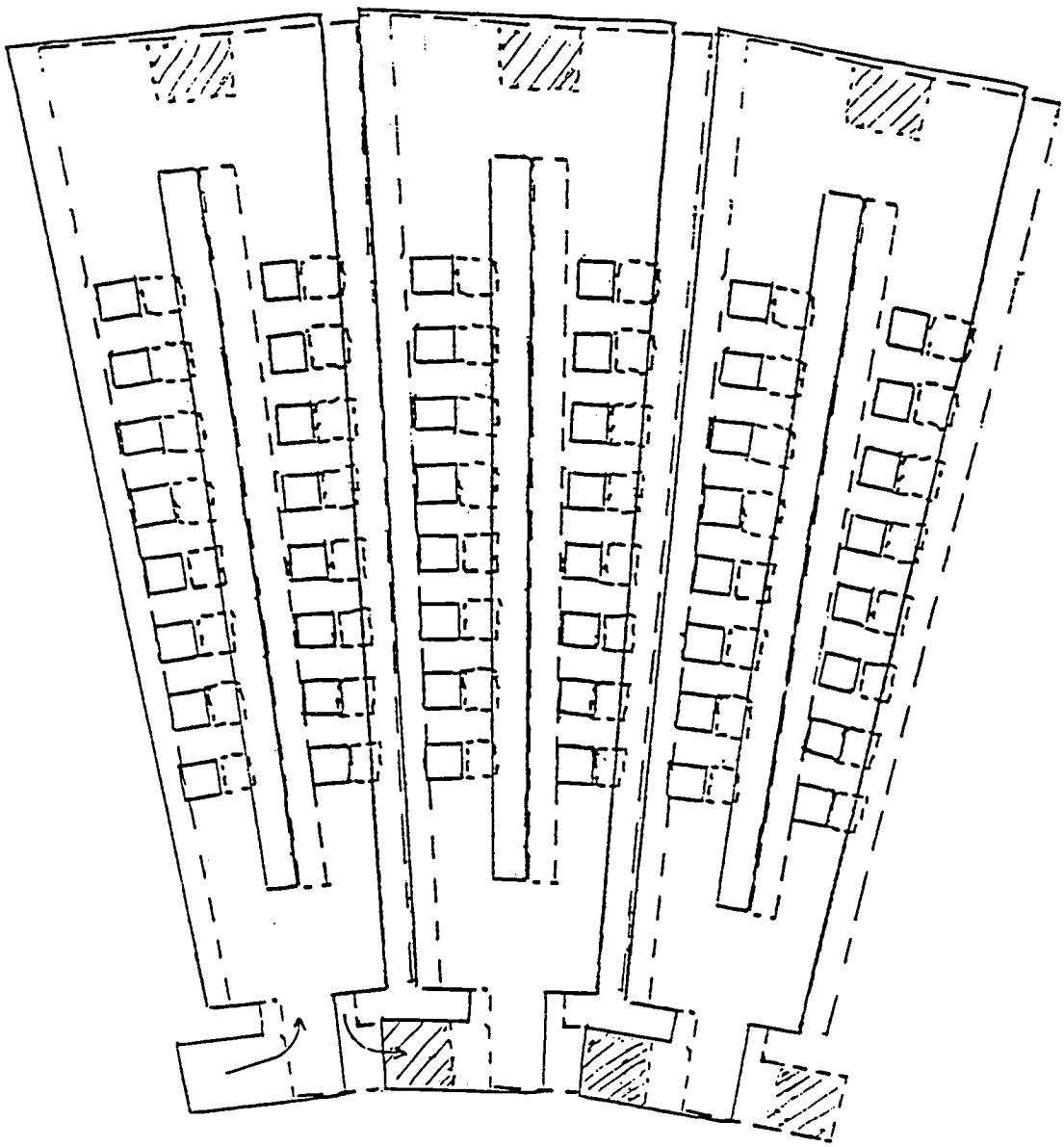
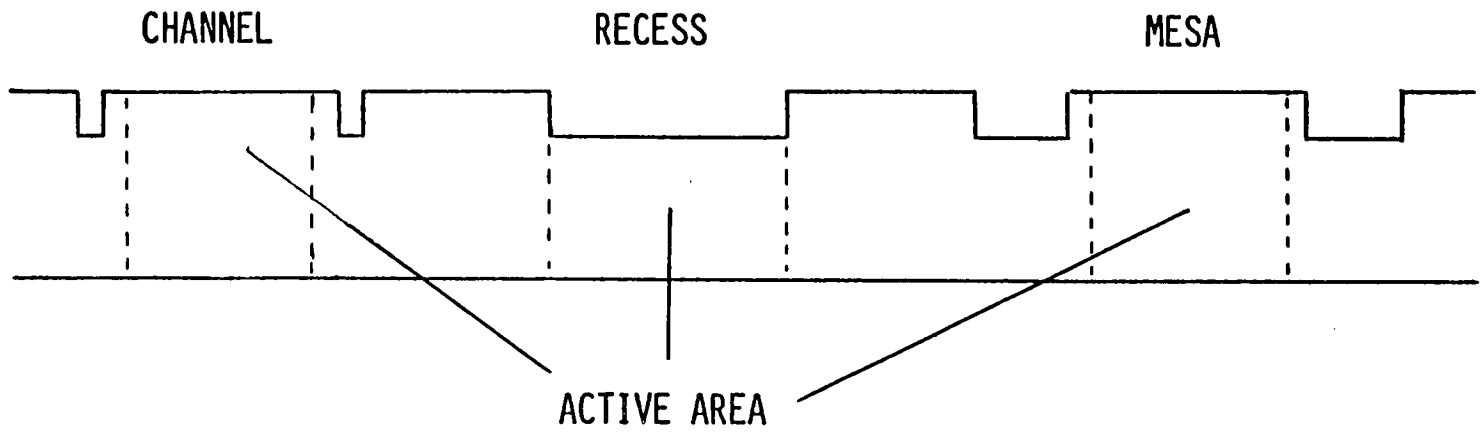


Figure 2.3.12 Three segments of Figures 2.3.10 and 2.3.11. This is an apertured current sheet together with its apertured ground plane (dashed). Another such pair is required for array propagation.




Cross section of various barrier structures.

Figure 2.3.13

## *2.3.6 I/O Tracks: Data Insertion and Removal from a Lattice

Three schemes for inserting or removing a row of bubbles from the lattice are shown in Figures 2.3.14, 2.3.15, and 2.3.16.

In Figure 2.3.14 the stripe propagation sheet is electrically connected to the I/O track. Bubbles will only propagate in that I/O track if the pulse pattern is a positive pulse 1+ in layer 1, then a negative pulse 1- in layer one, then a positive pulse 2+ in layer 2, then a negative pulse 2- in layer 2. Stripes will not propagate with that pattern. To propagate stripes the pattern must be 1+, 2+, 1-, 2-. This pattern will not propagate bubbles on the I/O strip. This approach has a disadvantage in that the I/O track propagator is the inferior type discussed in Section 2.3.1.

Figure 2.3.15 shows I/O track apertures that will propagate bubbles either vertically or horizontally depending on whether the current is horizontal or vertical. When that track is inserted into a stripe propagation sheet, the result is as shown. For stripe propagation the current is parallel to the I/O strip axis. For I/O, the current is perpendicular to the strip axis. This approach presents a difficulty in obtaining the I/O mode current direction when using a practical structure such as shown in Figure 2.3.10.

Figure 2.3.16 has separately accessed I/O strip in which bubble motion is parallel to the current direction. During I/O, there is current only in the strip. During lattice motion there is current only in the storage area. When lattice movement is taking place, the bubbles and stripes must get across the strip. It's expected that the force of the rest of the lattice will push the bubbles and stripes across the narrow I/O strip.

Of these approaches, Figure 2.3.16 appears to have the most advantages. It's possible to shift the I/O track's second apertured conductor to the right in addition to down as used in 2.3.16. This shift to the right will aid propagation of the lattice across the I/O strip, if self-structuring alone is inadequate pushing across the strip.

These I/O strip designs can be designed to remove several columns of bubbles at once, or to have bubbles going around in an I/O loop.

## 2.3.7 Bubble Generation

There are two basic designs for bubble generators incorporated with apertured dual conductor propagation devices. One design requires a third conductor level,

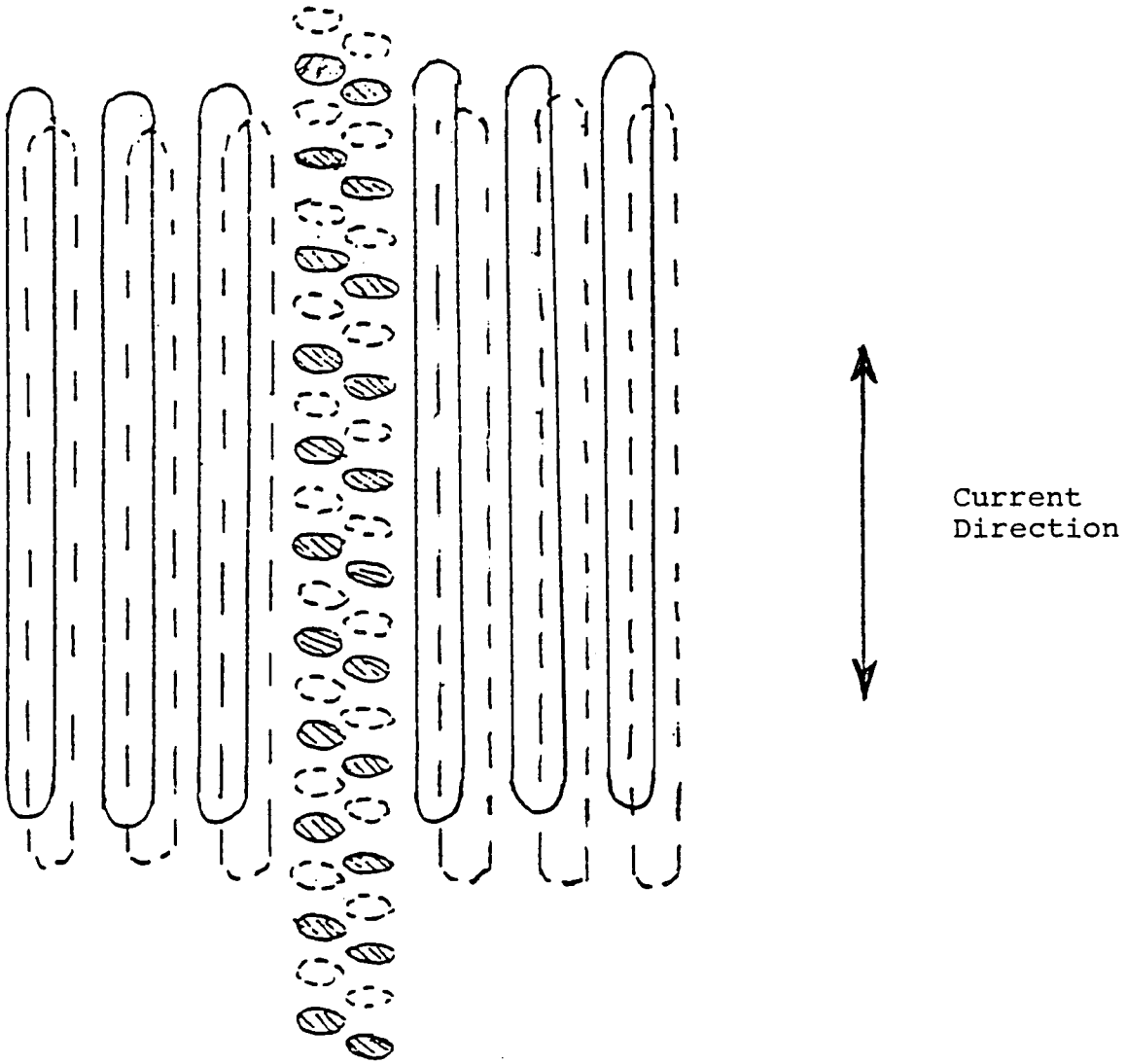



Figure 2.3.14 Stripe propagators and bubble input/output track. For stripe propagation, the pulse pattern is 1+, 2+, 1-, 2-. For I/O, the pattern is 1+, 1-, 2+, 2-.

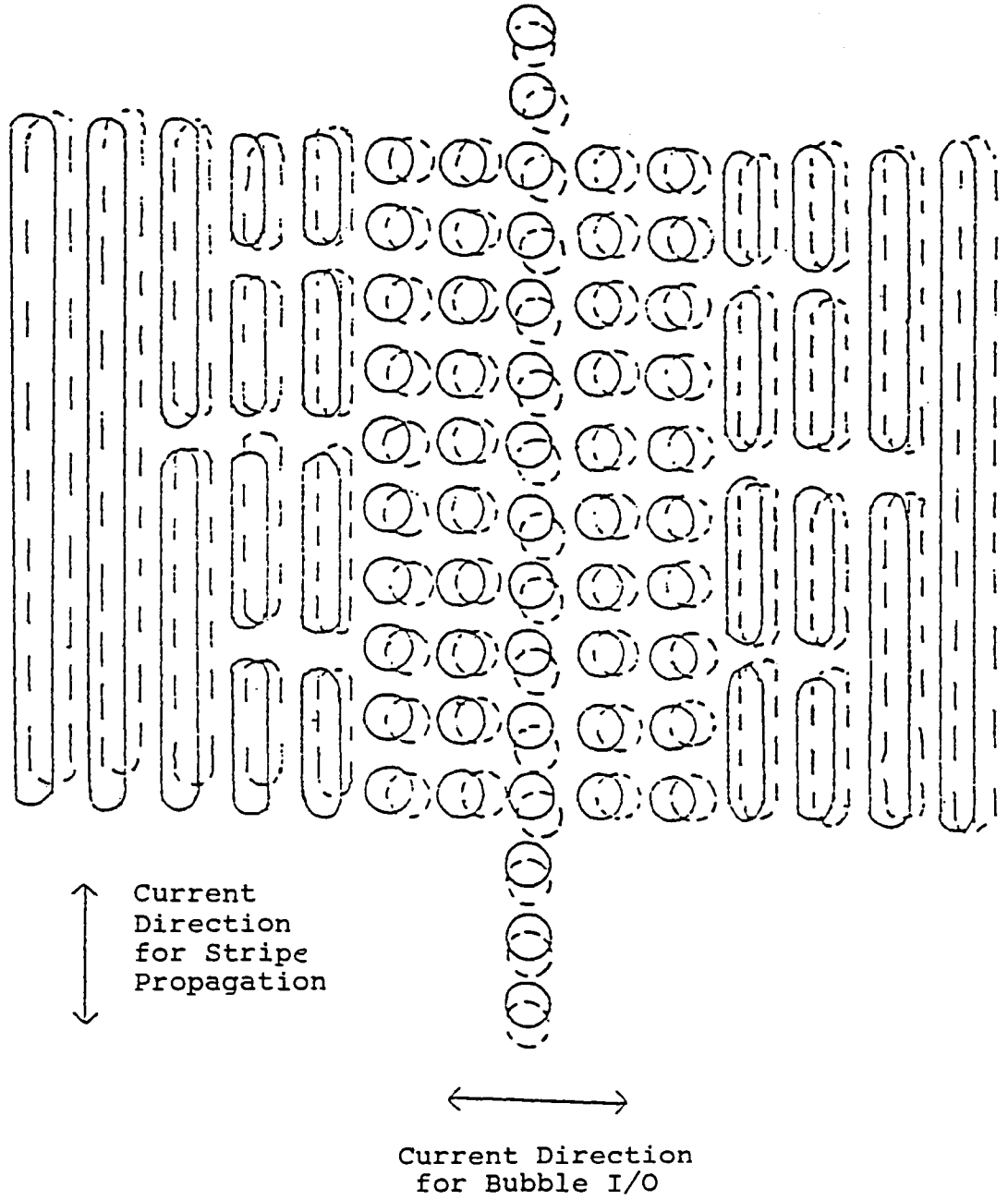



Figure 2.3.15 Stripe propagator with I/O for a row of bubbles.

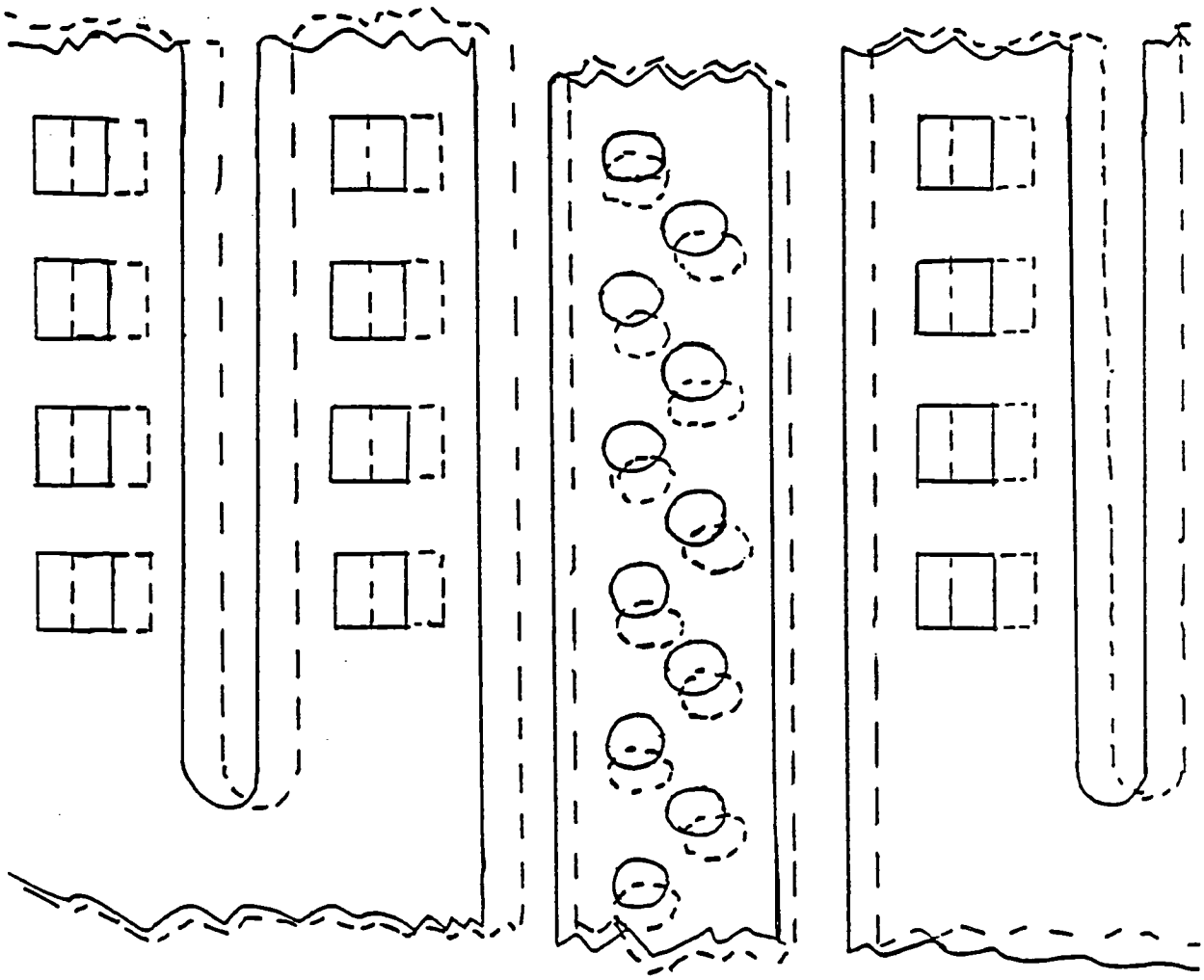


Figure 2.3.16 I/O strip preferred design.

and employs the familiar hairpin structure. The second design has the generator patterned in one of the propagation conductors, and requires a change in current magnitude and/or direction to generate a bubble domain.

Third Level Conductor - A bubble generator in a third conductor level can have two basic geometries, as illustrated in Figure 2.3.17. The (a) design is very common, and the (b) design has the generator section directed oppositely to the first design. The (b) design could be used when it is desired to remove a bubble from the generator and not pass it under the conductor.

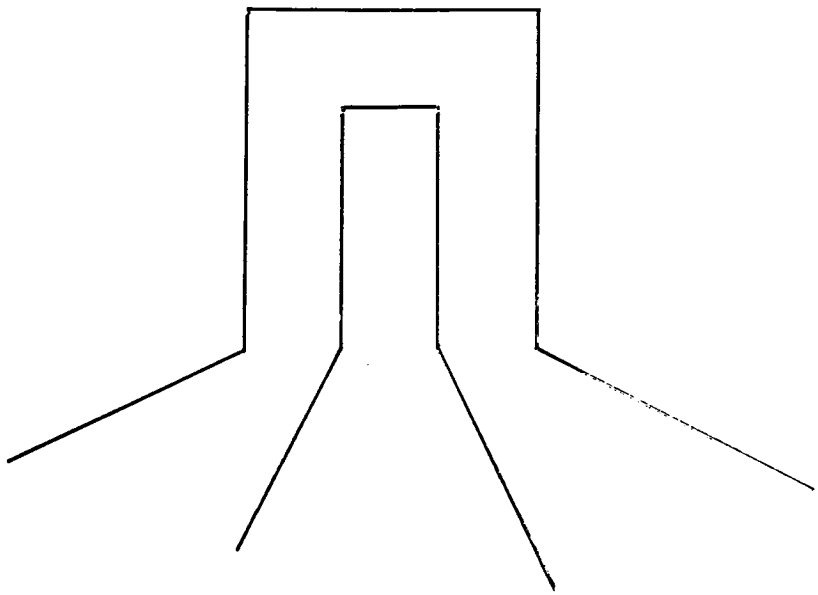
Magnetic field measurements from scale models of the (a) design, and observations of bubble generation in actual circuits, have demonstrated that the maximum normal field is located approximately 15% of the leg width away from the closed end conductor. This value is dependent on the separation between the conductor and the point in question. Conductor widths and spacings should be near two microns in dimension for the bubble density required in this memory design.

Propagation Levels - A bubble generator patterned in one of the two propagation conductors can have two different designs. Figure 2.3.18 illustrates a design where a normal propagation aperture has been modified with a long aperture oriented orthogonal to the normal aperture. Application of a current orthogonal to the propagation current will generate a magnetic dipole defined by the long apertures.

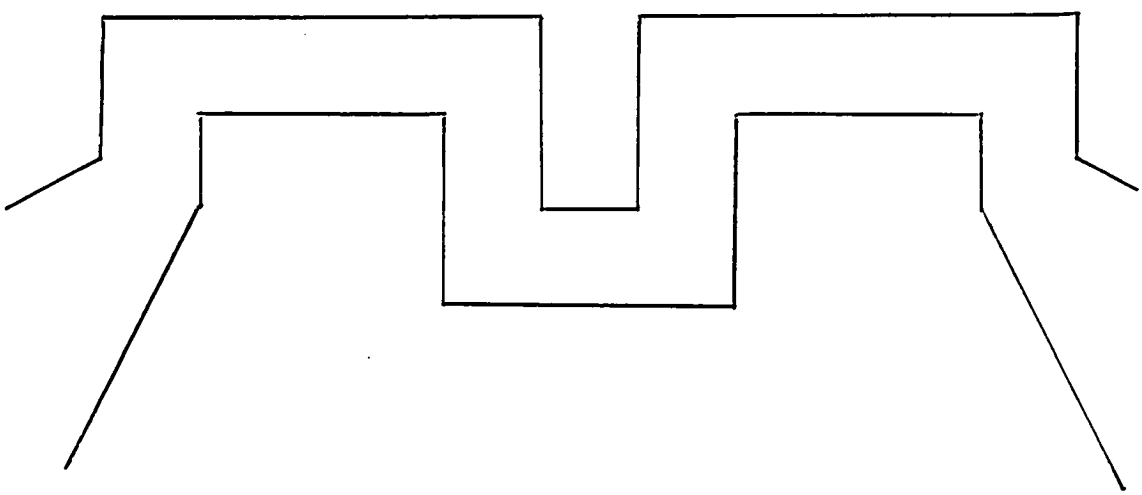
A second design incorporates a long slot in one propagation conductor, as illustrated in Figure 2.3.19 [ 2 ]. Current is concentrated between the end of the slot and a normal propagation feature, and will generate a bubble where the current density is large. A current pulse, in addition to the current pulses employed for bubble propagation, is required for bubble generation.

Each of the bubble generator designs requires a large current density in the conductor. This is especially true when the generator is located in a third conductor layer, where the additional separation between the garnet and conductor requires higher current levels to overcome inefficiency in field generation. Reducing the duration of the current pulses becomes most important, and reliable operation at 20 nsec has been reported for contiguous disk devices [ 3 ]. As the bubble diameter decreases, the resultant current density in the generator increases, due mainly to the large increase in nucleation fields dictated by the garnet properties: $H_N \propto H_K - 4\pi M$. By having a larger bubble diameter for a given data density, the self-structured device reduces this current density compared to a conventional non-self-structured device.

(a)



(b)



Two hairpin design bubble generators.

Figure 2.3.17

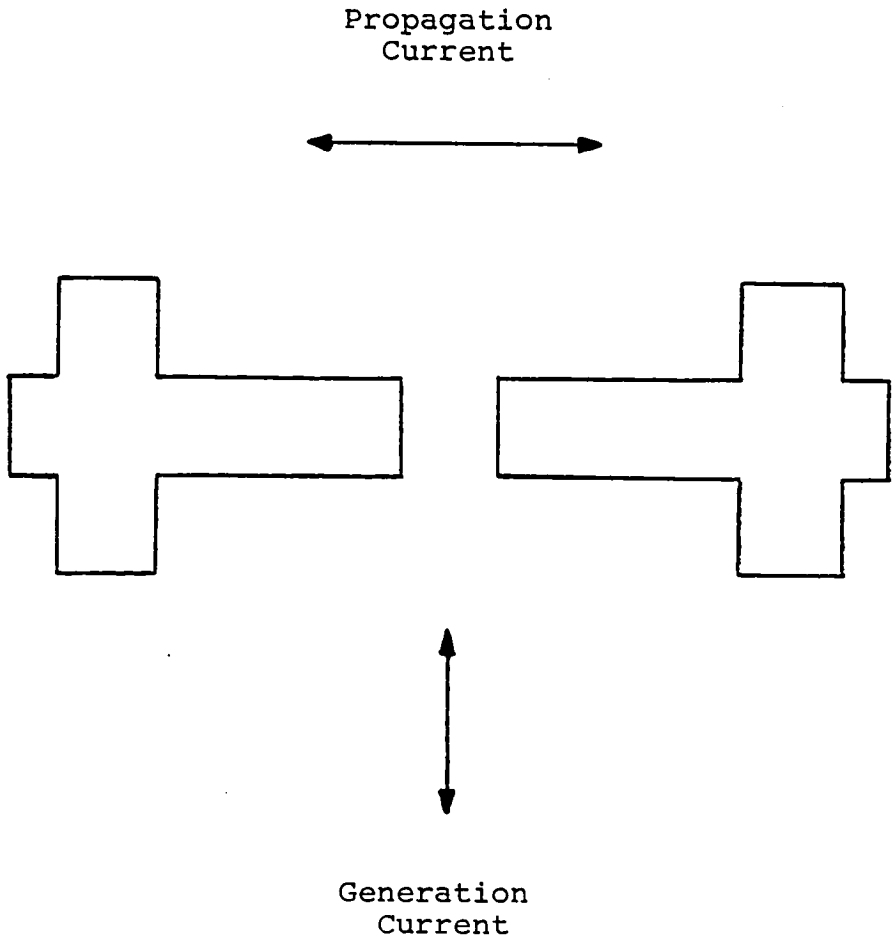



Figure 2.3.18 Modified conductor apertures for bubble generation.

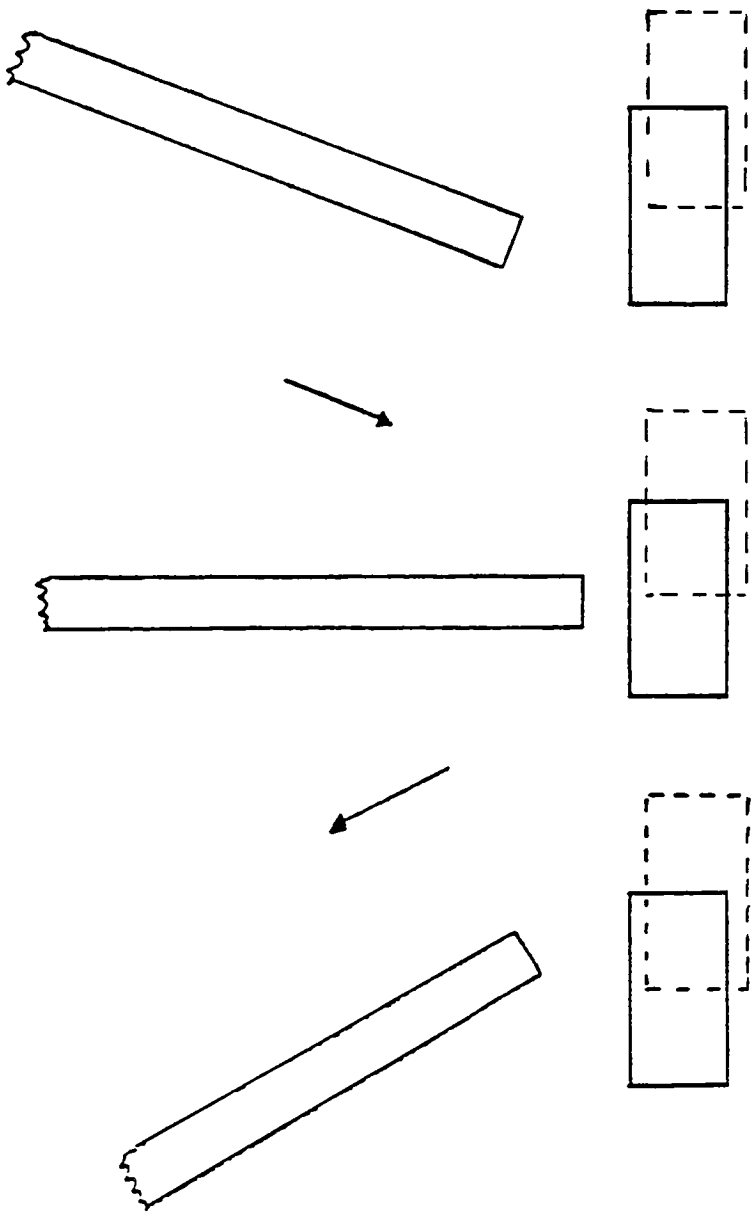


Figure 2.3.19 Channeled current for bubble generation near propagation apertures.

## 2.3.8 Gating:

### Transfer gates:

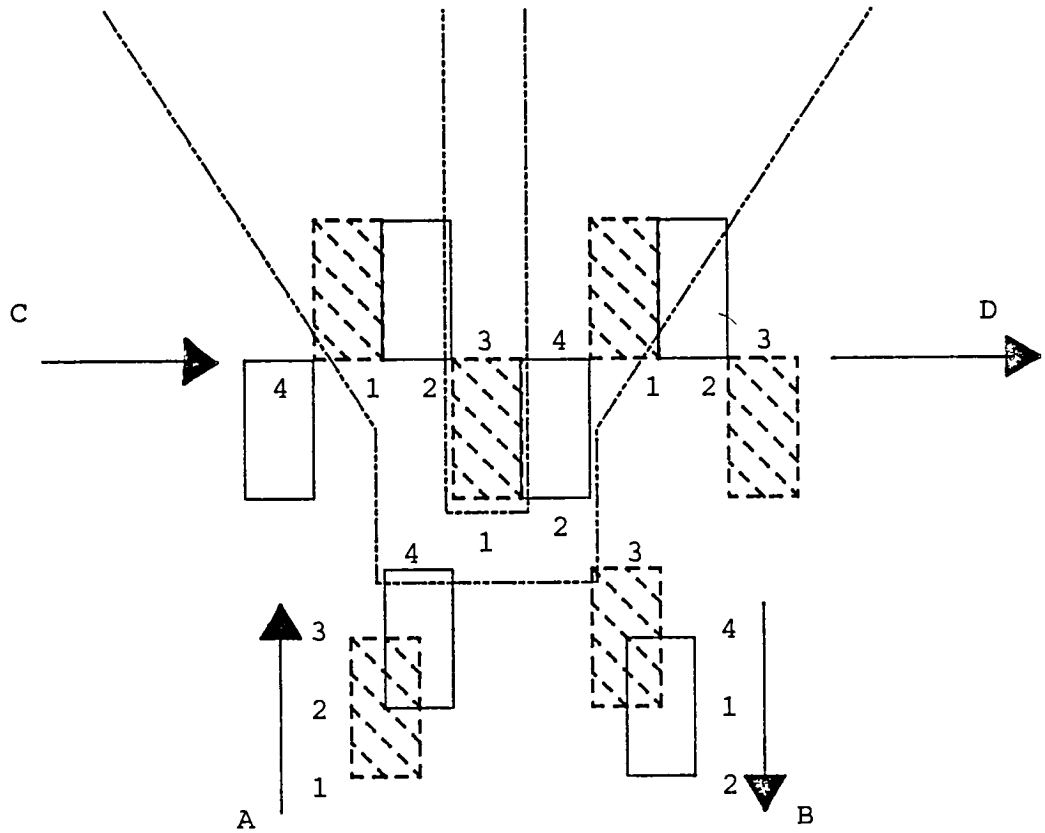
Transfer of bubbles appears feasible with two different approaches compatible with apertured conductor propagation. One approach is to use a third level transfer conductor to either hold the bubble at a location, or strip it between locations in ways that divert it to the desired energy well provided by the apertured conductor propagation. A second approach provides the transfer function using only the two propagation conductors. Examples of each will be covered next.

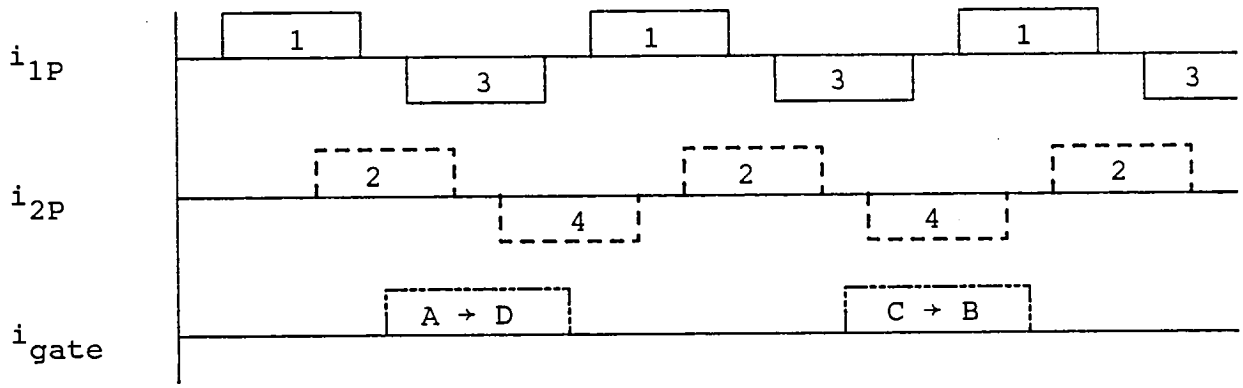
Figure 2.3.20 shows a third level hairpin control conductor and the necessary drive pulse timing to provide a transfer in or a transfer out of a bubble between a storage loop end and an I/O track. A bubble coming up 'A" in the figure is prevented from continuing around the end of the storage loop by pulse 'A → D'. The bubble is held at a position within the hairpin until the '3' pulse is applied and the overlapping '2' pulse has ended. The combination of the attractive region within the hairpin, the repulsive pole at the '1' end of the aperture within the hairpin, and the attractive pole at '3' at the same aperture results in the bubble moving to '3' and then continuing down the I/O track (→D) with the ending of the hairpin pulse and the application of propagation pulse '4'. Similar operation using pulse 'C → B' results in a transfer of bubble into the storage loop from the I/O track.

Figure 2.3.21 shows another bidirectional, third level conductor transfer gate. This approach uses an aperture in the conductor to provide the holding field. As shown by the timing pulses, the operation is similar to the Figure 2.3.20 gate with a transfer pulse 'A → D' moving a bubble out of the storage loop into the I/O track and a pulse 'C → B' doing the reverse.

Figure 2.3.22 shows an 'N' transfer gate [12] again using the third level conductor. This structure provides a uni-directional transfer function with Figure 2.3.22 showing a transfer-out geometry and pulse timing. A mirror-imaged gate provides a transfer-in function.

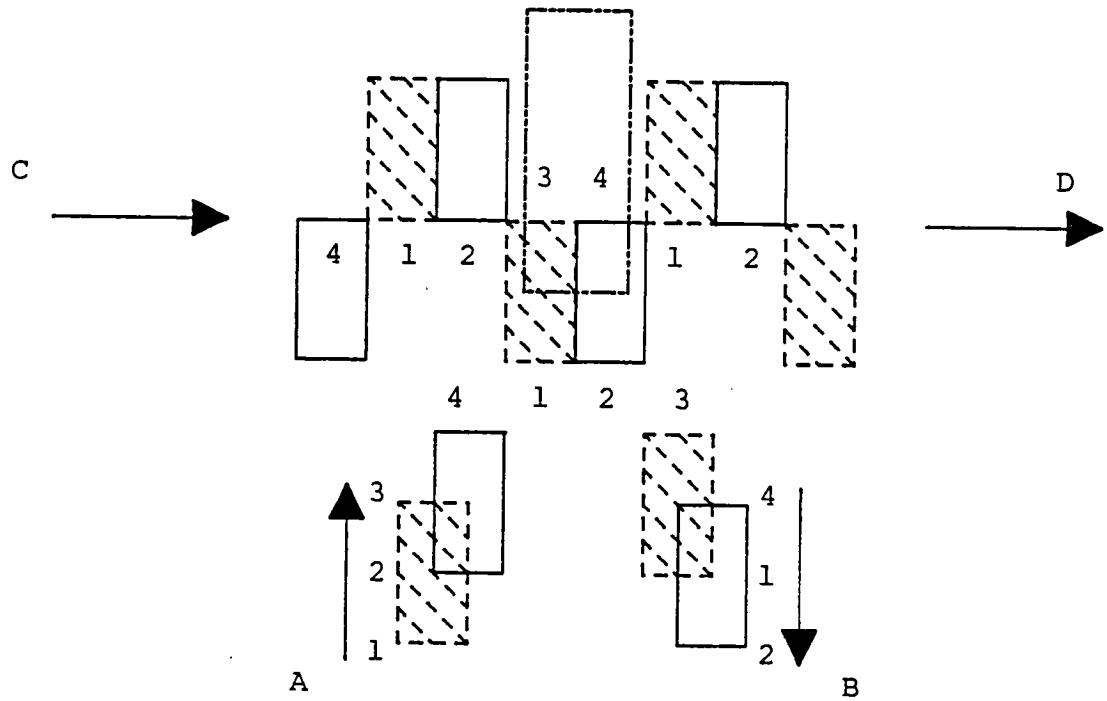
An example of a transfer function provided by the propagation conductors is shown in Figure 2.3.23 [ 2]. In this gate, bidirectional transfers occur as a result of modified apertures and modified current pulse sequences as shown. A regular sequence of pulses, 1, 2, 3, 4, 1, etc. causes the bubble to propagate around the loop from position A to B. A variation in the sequence, 1, 2, 1, 4, 1, 2, 3, 4, 1, etc. causes the bubble to cross the

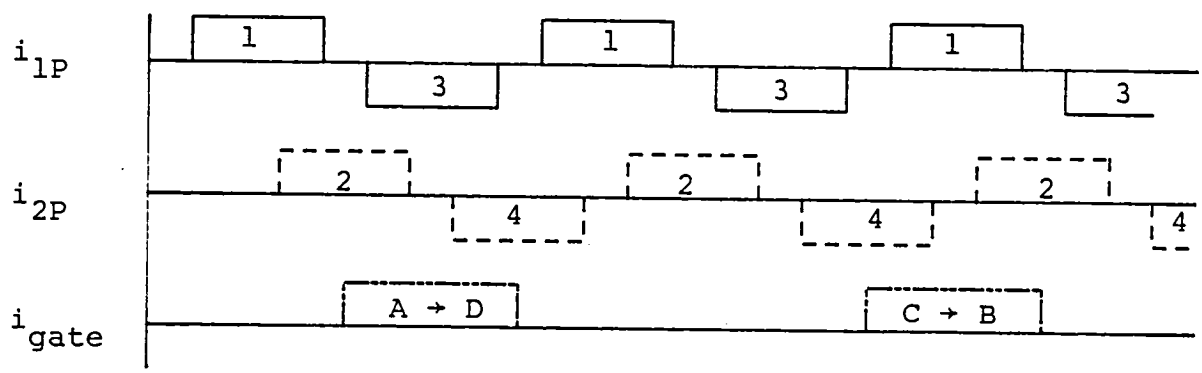



Transfer gate using third-level hairpin control conductor

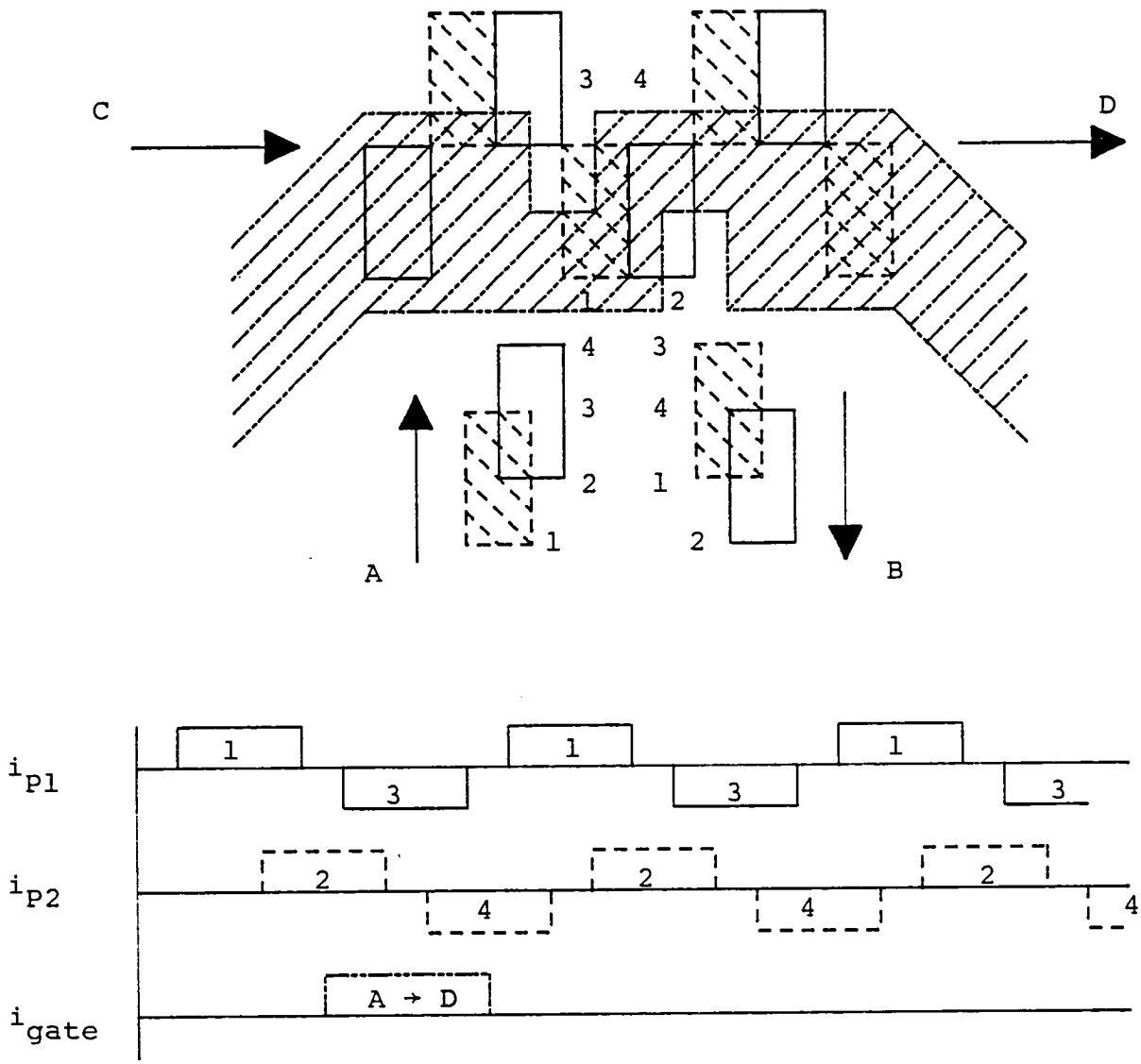
Figure 2.3.20



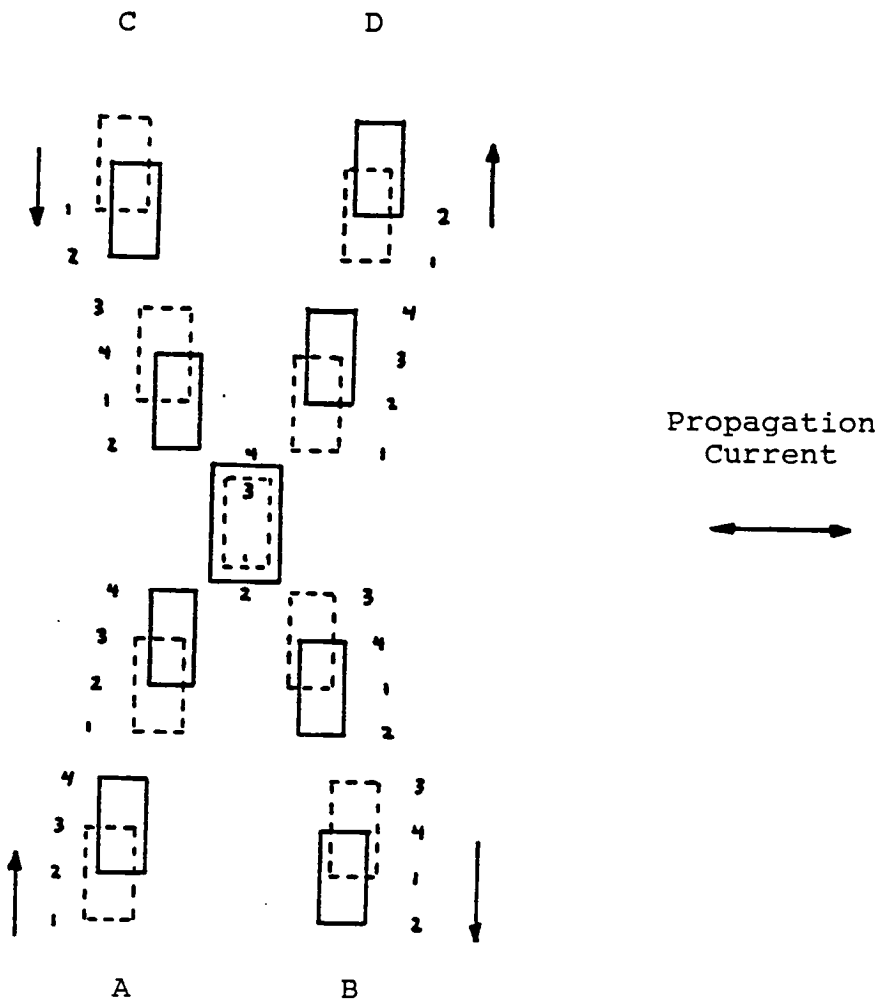

Bi-directional transfer gate using apertured, third level control conductor.

Figure 2.3.21




'N' Transfer-out gate using third level control conductor.
Bubbles go from 'A' to 'D' when transferred.

Figure 2.3.22




| | | |
|---|---|---|
| | 1 2 3 4 1 2 3 4 1 2 3 4 gives A → B + C → D | |
| Sequence | 1 2 3 4 1 2 1 4 1 2 3 4 gives A → D | |
| | 1 2 3 4 3 2 3 4 1 2 3 4 gives C → B | |

Figure 2.3.23 Transfer gate employing modified current sequence and only propagation layer conductors.

transfer gate, utilizing the nested apertures, and proceed to position D. A sequence 1, 2, 3, 4, 3, 2, 3, 4, 1, 2, etc. causes the bubble to be transferred from 'C → B'. Bubbles that are not in the transfer position are not affected by the pulse sequence changes, but only idle forwards and backwards. When normal propagation resumes, the proper stream of data has been retained.

Merge Gates:

Merge gates which enable bubbles to be funneled from two or more I/O tracks down to one are shown in Figure 2.3.24. 'a' shows the merging of two tracks perpendicular to the current flow into one. 'b' shows the merging of two tracks parallel to the current flow into one. 'c' shows a modification of b's function and also a merging of one track perpendicular to the current flow and one parallel, into an output parallel to the current flow direction. All of these merge gates work properly for only one direction of propagation. By using a third level control conductor, these gates could be operated as a switch if the bubble propagation direction was reversed.

Swap Gates:

Swapping of bubbles between an I/O track and a storage loop appears feasible using third level control conductor.

A swap gate is illustrated in Figure 2.3.25 where control conductors are employed to transfer the bubbles between two data tracks. The control conductors are energized after propagation pulse 1, causing the bubble to strip-out between the conductor legs. This current remains on until propagation pulse 3 is applied, and then is turned off. The stripe will collapse to a bubble at position 3 on the opposite track, and the swap is complete. Because of the two tracks propagating in opposite directions, the swap function does not result in any data delay. Two concerns, however, are that the third level conductor doesn't meet the minimum feature size criteria if the propagation apertures just do, and the stripping distance requires a higher velocity than the normal propagation if no accommodation is made in the propagation pulses at the swap time.

Another control conductor swap gate is shown in Figure 2.3.26. With no control conductor current applied, bubbles in the storage loop travel up 'A' and down 'B' and the bubbles in the I/O track travel from'C' to 'D'. If the control conductor pulses are applied as shown in the figure, then the paths of the two bubbles being swapped are as shown by the heavy line. The two bubbles are sequentially

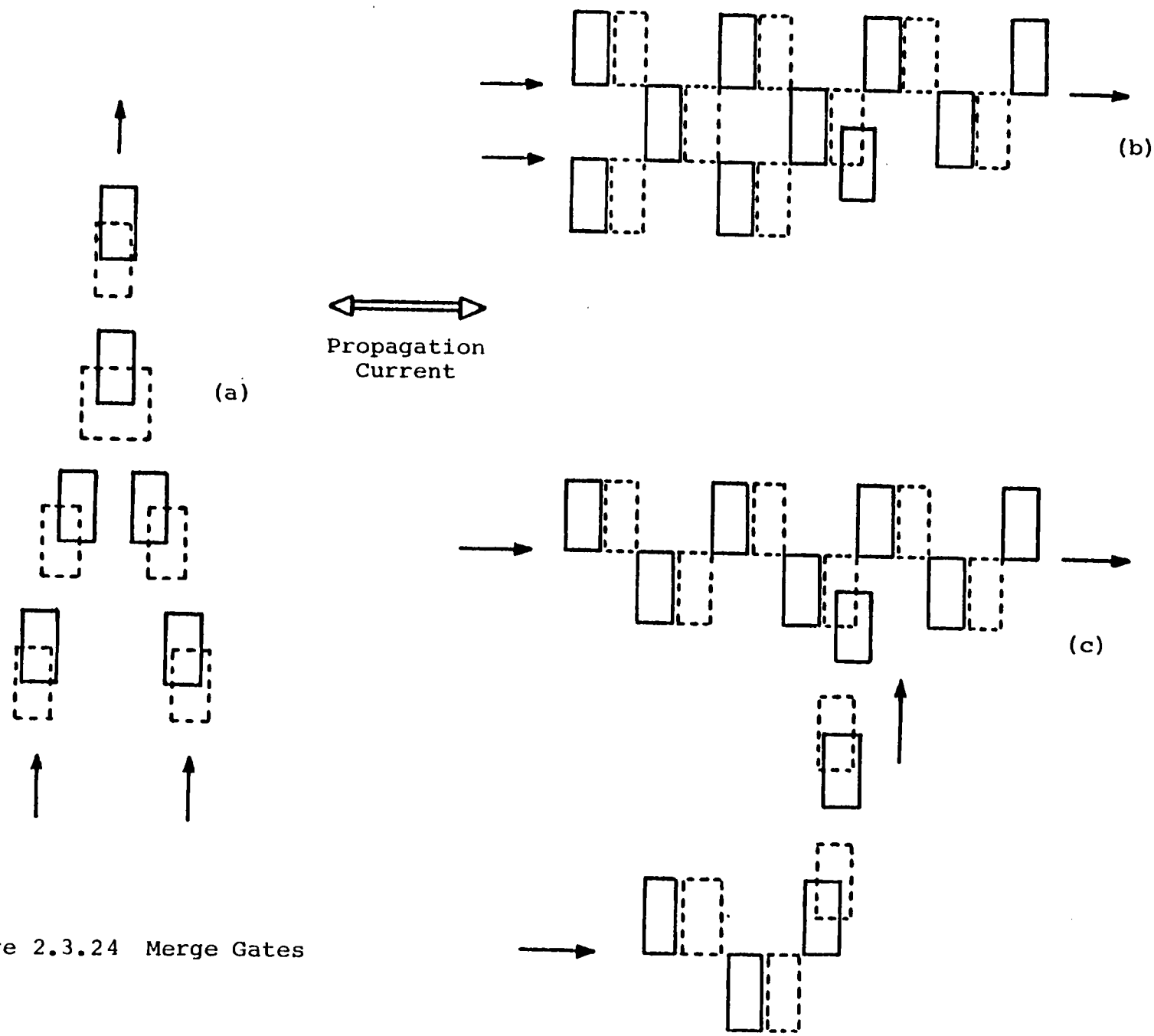
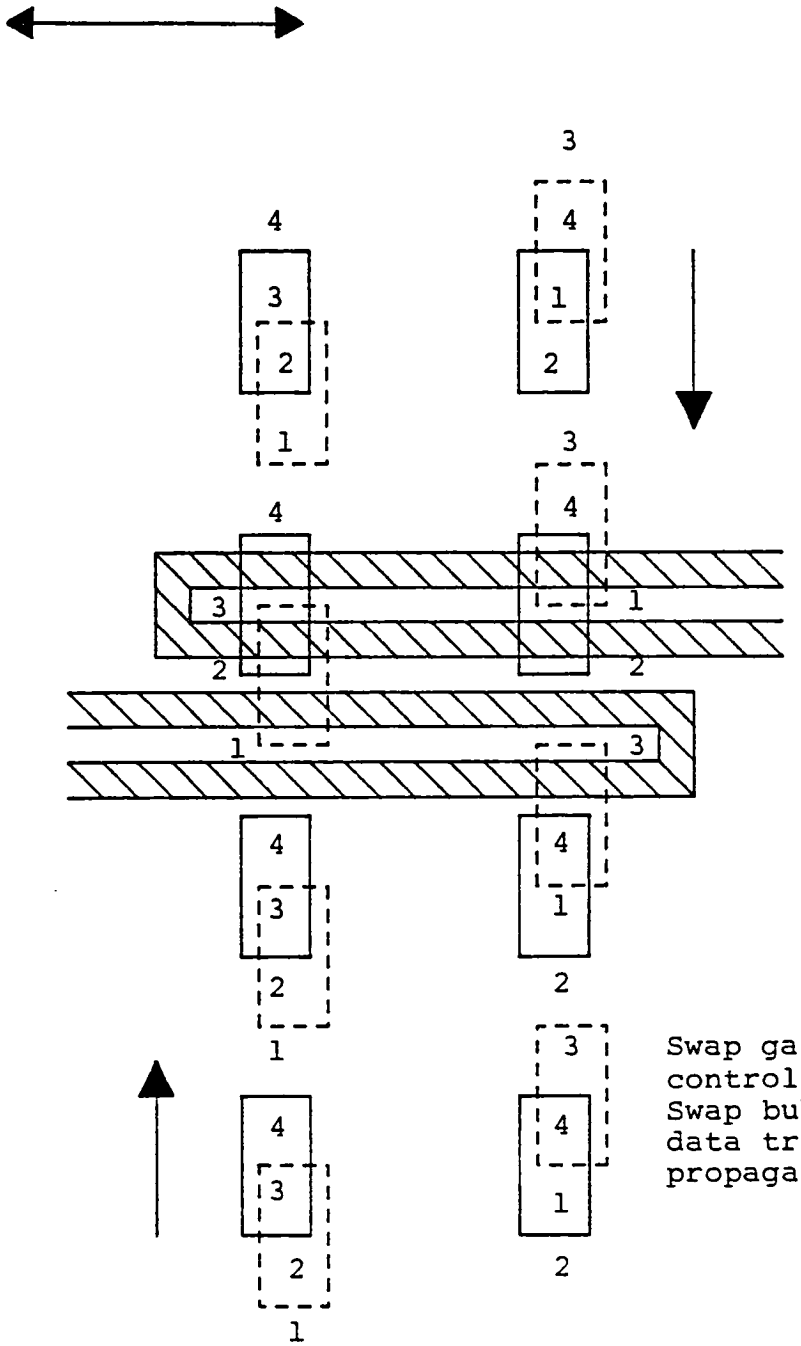



Figure 2.3.24 Merge Gates

Propagation Current



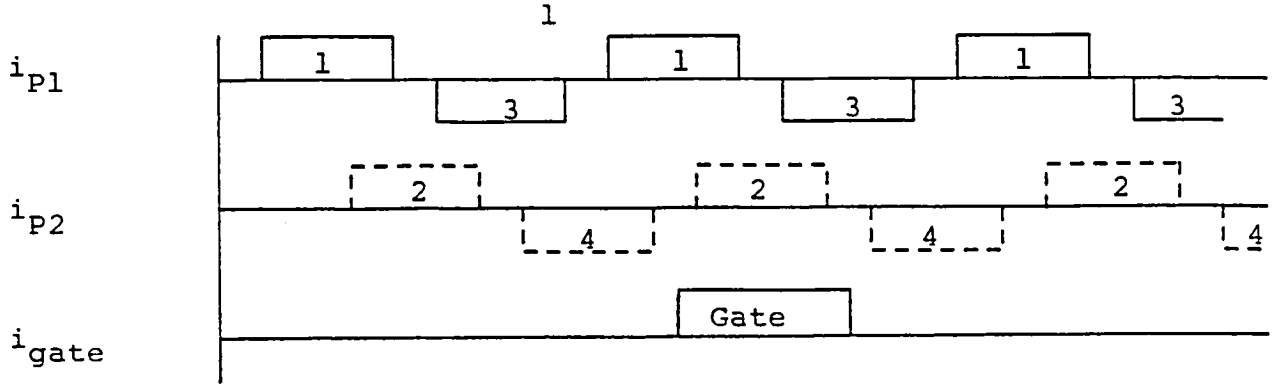




Figure 2.3.25

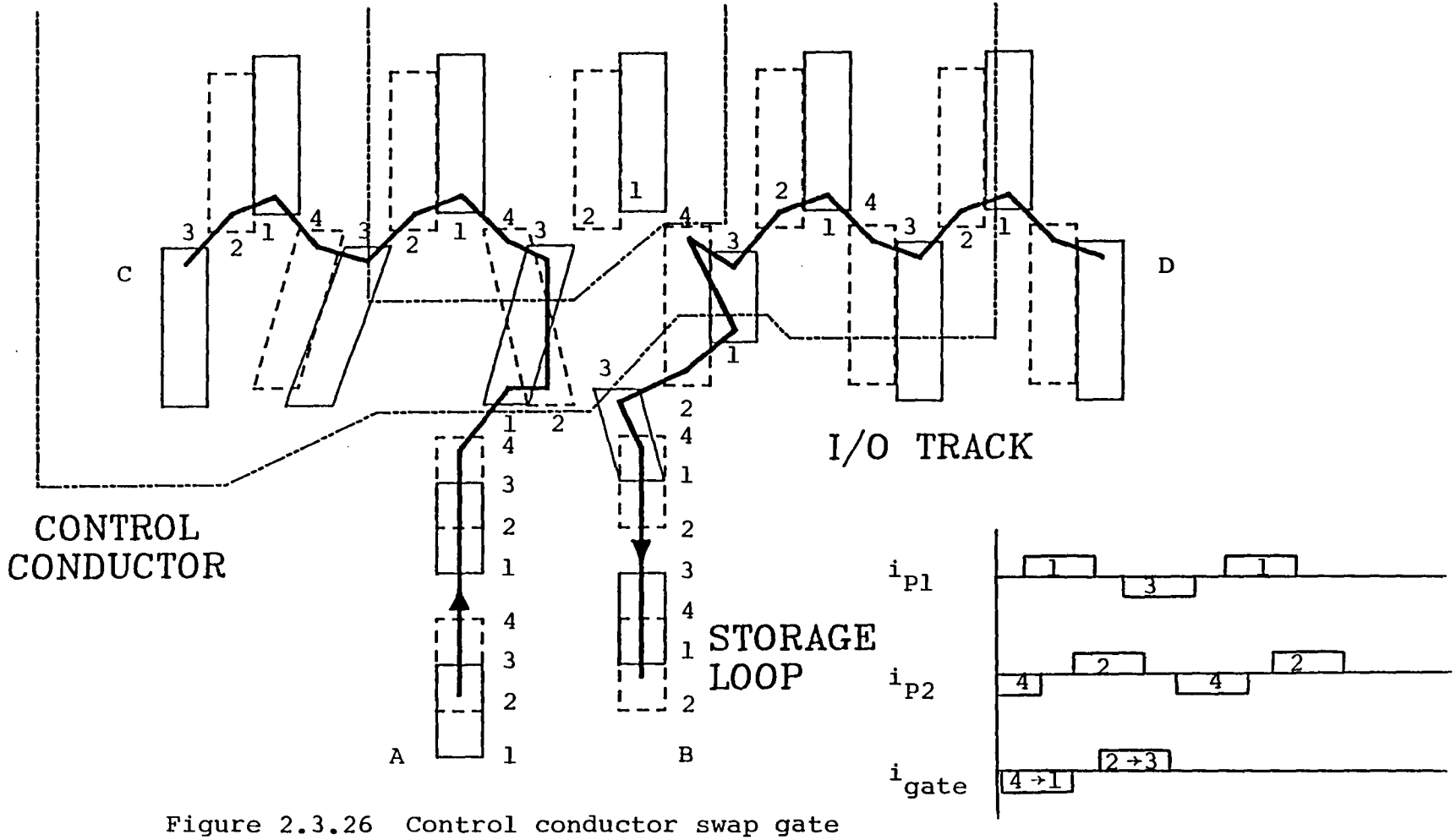



Figure 2.3.26 Control conductor swap gate and drive pulses

transferred by the two control pulses with the result being a swap which preserves phase and doesn't delay (or idle) other bubbles in the chip.

Replicate Gates:

A bubble replicator gate is illustrated in Figure 2.3.27. A region of the garnet is heavily ion implanted, which results in a lower bubble collapse threshold than the rest of the garnet. The bubble at position '1' on the slanted apertures is caused to strip-out between the legs of control conductor loop with a current pulse at time slot 1. A short reverse pulse in the control loop will cut the stripe domain into two segments, and the segments collapse to two bubbles, resting at position '1' on the 'C' to 'D' path between the legs of the loop, and also at the '1' end of the slanted aperture. This completes the bubble replication operation. Bubble replication can also be initiated with a bubble at position '1' in the 'C' to 'D' path inside the control loop.

Another replicate gate, similar in operation to Figure 2.3.27 but without the ion-implantation, is shown in Figure 2.3.28. In this approach, the non-uniform field generated by the third-level control conductor cuts the stripped-out bubble.

A difficulty with bubble replication in general and specifically in the two designs just presented is that stripping of the bubble so that it can be cut either requires a higher stripe head velocity than the general propagation velocity or else requires the propagation to be slowed during the replicate time interval. To maintain maximum device performance, the second alternative is preferred. One approach to implement an effective propagation slowdown is to cycle the propagation pulses through an 'idle' sequence such as -1-4-1-2- with timing as shown in Figure 2.3.29. This permits maximum operating speeds when moving bubbles in the I/O track and storage loops without having to change the fundamental propagation clock frequency. Another approach is to do a logic divide by two or divide by four of the clock rate while the control conductor pulses are applied. This would be a simple capability to supply in the controller hardware.

## 2.3.9 Detectors

The detection approach of interest is magneto-resistive sensing of bubbles or stripped bubbles using thin film Ni-Fe. It's expected that these current access devices have a sensitivity advantage compared to conventional

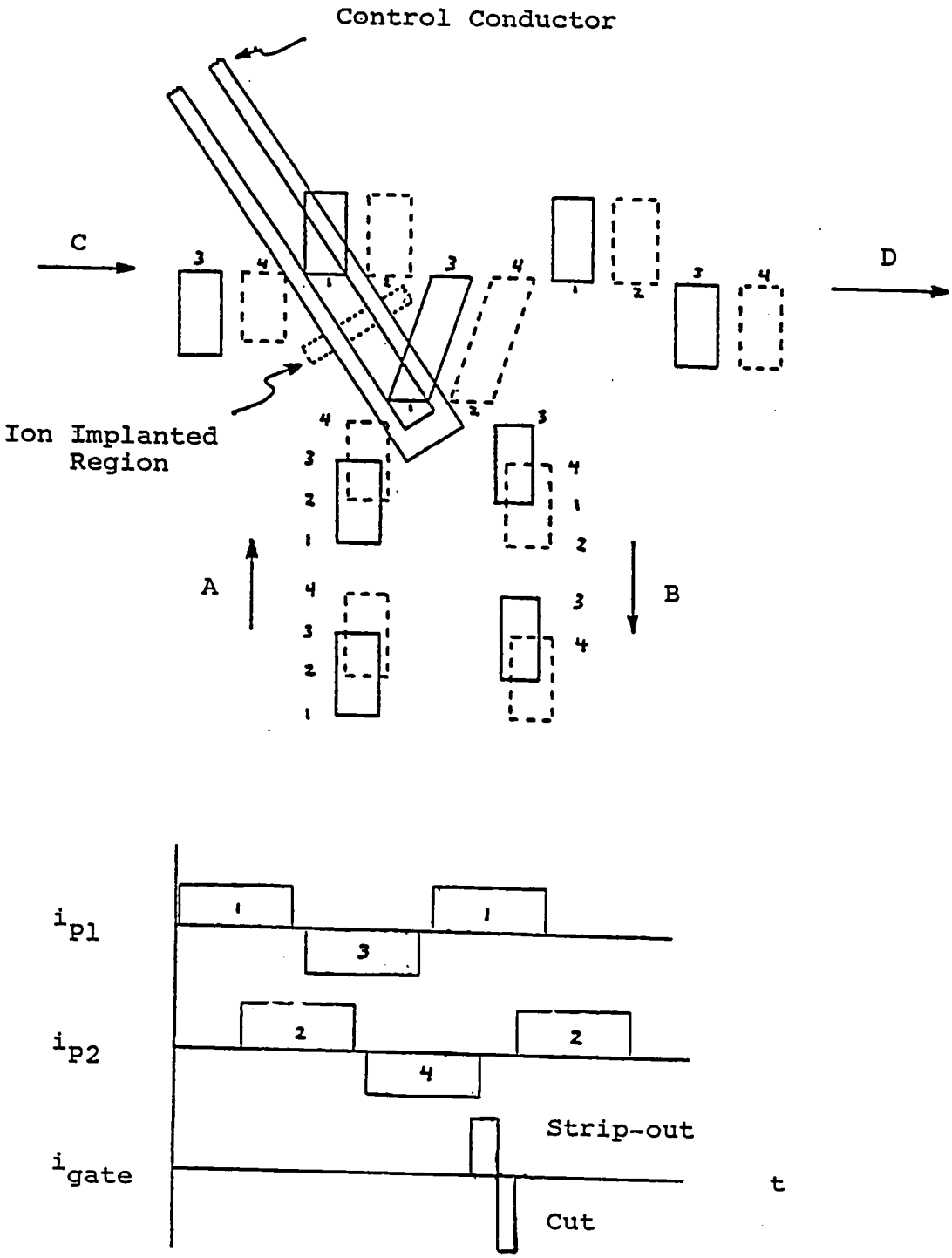
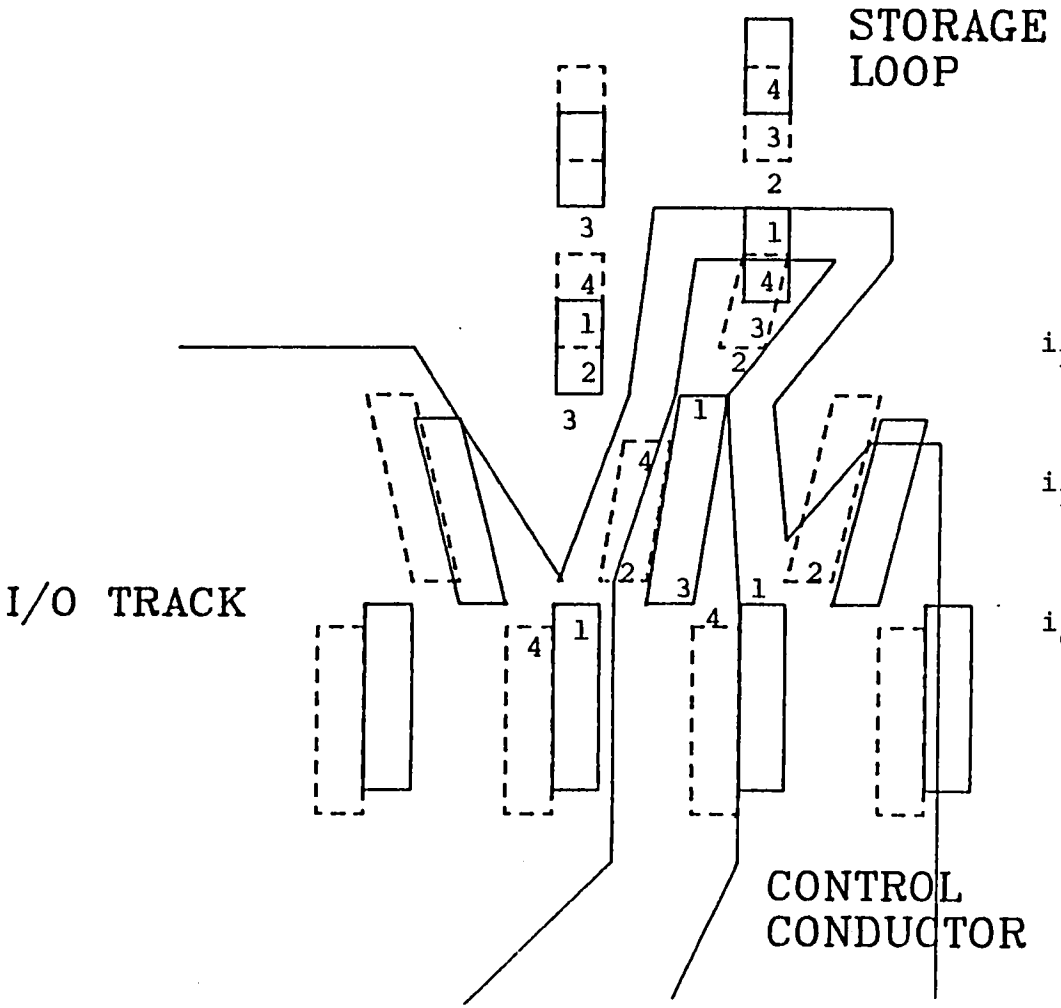
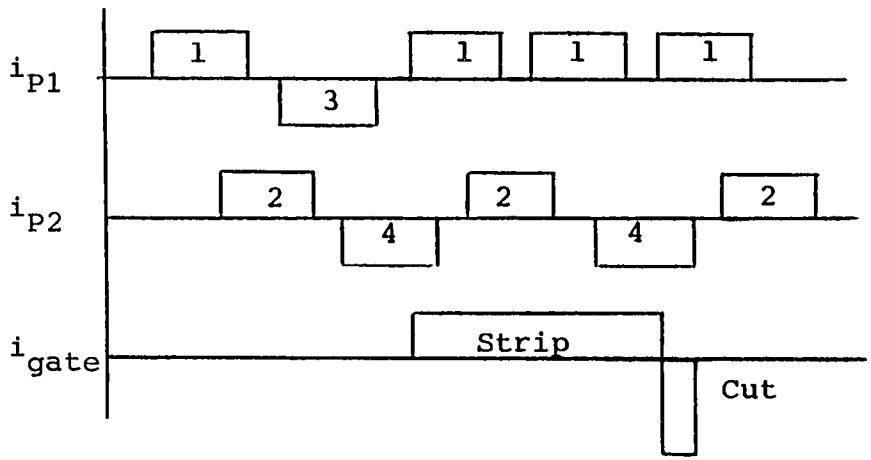



Figure 2.3.27 Bubble replicator gate using third level control conductor and ion-implanted region.




Control condutor replicate gate using non-uniform generated fields to strip and cut a bubble.

Figure 2.3.28




Idle propagation pulse sequence provides time for stripping pulse to expand bubble.

Figure 2.3.29

Ni-Fe propagation element, field access devices. One advantage results from the Ni-Fe detector deposition being just that, a detector deposition, and not a propagation element deposition with the detector included. This means that the Ni-Fe parameters such as anisotropy thickness, $\frac{\Delta\rho}{\rho}$, and coercivity can be optimized for the detector needs.

In particular, thin film detectors of 350A° thickness can be used instead of the roughly ten times thicker material used when fabricated from the propagation deposition. The thinner material gives a greater $\Delta R$ change in resistance when switched and therefore a larger signal voltage for a given bubble stretch. A second advantage of the current access approach is that the rotating field and rotating field sensitive propagation elements are eliminated, and thus if desired, in-plane DC bias fields can be applied to the Ni-Fe detector to provide an optimum operating point.

Figure 2.3.30 shows a design for detecting bubbles without stripping. As shown, thin film Ni-Fe elements are present on both sides of the bubble path. In operation, the shape and growth anisotropy characteristics of the Ni-Fe align its magnetization along the direction of the detector current flow if there is no bubble present. This can be aided by the weak in-plane fields ($\sim$10 Oe) from the propagation conductors if no return conductor is used. When a bubble is present between the Ni-Fe elements, the in-plane component of its stray fields switch the magnetization of both Ni-Fe elements to be orthogonal to the detector current flow. As shown, a 'dummy' detector for maximum signal to noise ratio is planned.

Figure 2.3.31 shows a detection structure which does strip out bubbles. Because of the 1.5 MHz data rate requirement, it is not possible to quickly expand the bubble into a long stripe domain. With each step of the propagation/domain-expansion current pulses, each end of the expanding stripe domain will move sideways approximately the same distance as the bubbles forward propagation. The domain stretch velocity is limited by saturation mobility. For example, if a bubble is to be expanded into a stripe with a width 50 times the bubble diameter, approximately 25 expansion steps will be required and at least as many contraction steps. This demands an appreciable area on the chip, but is necessary if a stripping approach is taken. In Figure 2.3.31 the current is perpendicular to the propagation direction. On the input side, the propagation apertures become long slots which strip the bubble before it reaches

# DETECTION WITHOUT BUBBLE STRIPPING

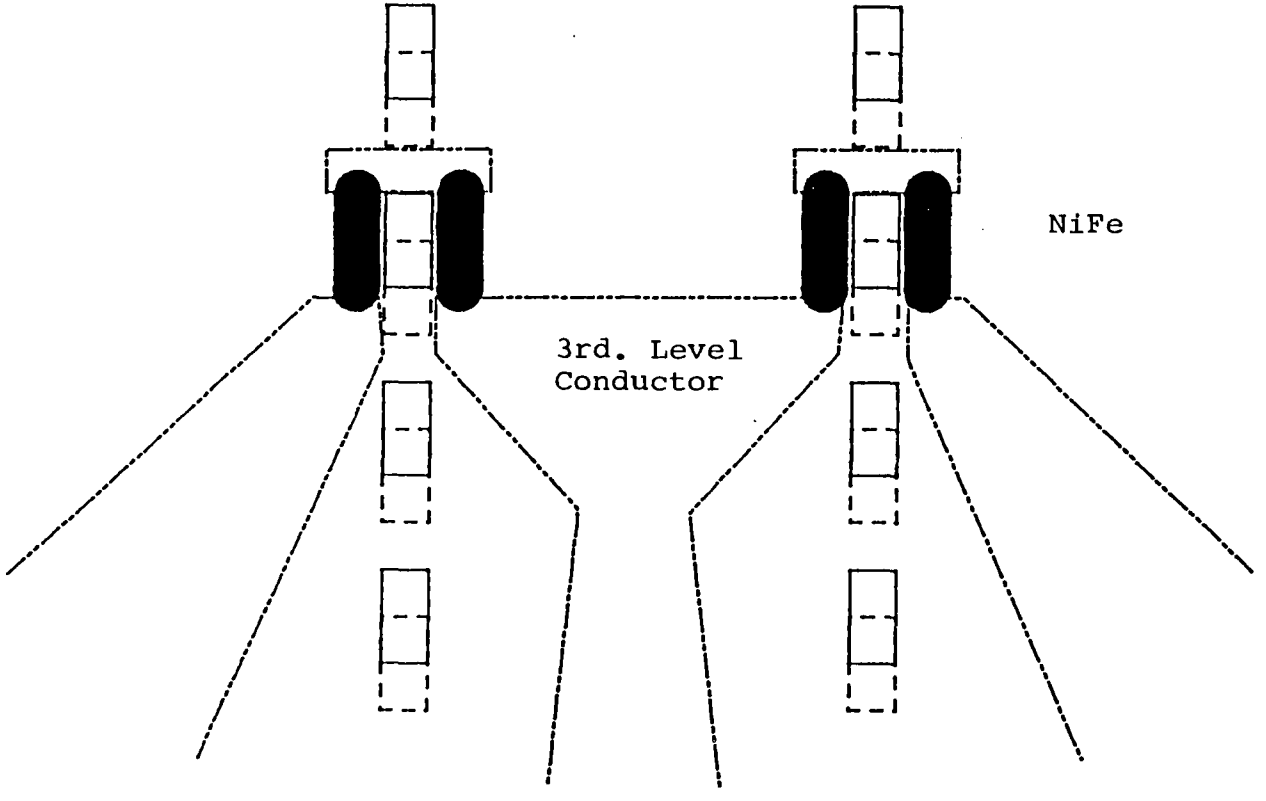



Figure 2.3.30

# DETECTION WITH BUBBLE STRIPPING

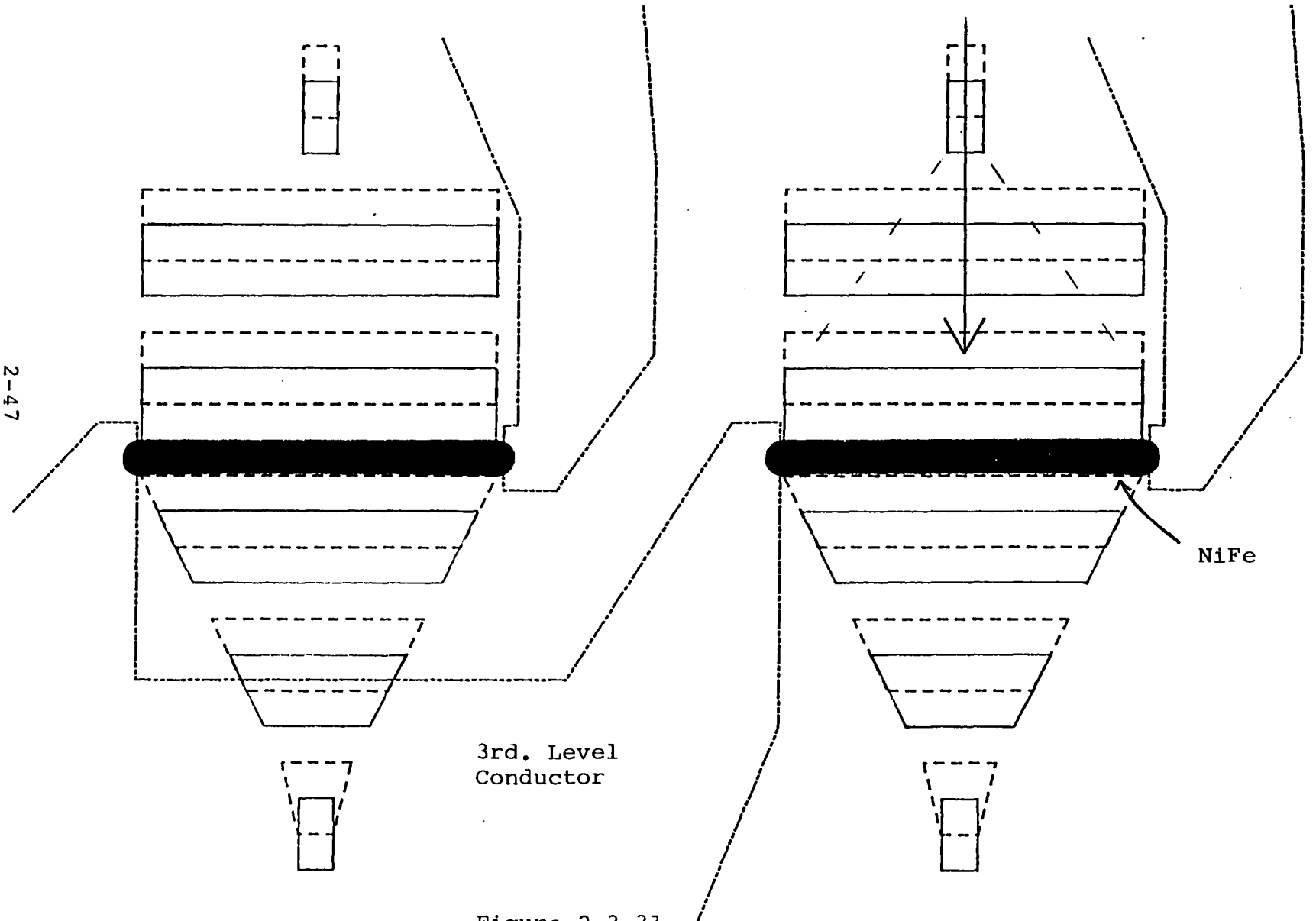



Figure 2.3.31

the Ni-Fe element. Once past the detector, the propagation slots taper down gradually to collapse the stripe back into a bubble or alternatively, collapsing it entirely. Note that this tapering region is needed even in the destructive read-out mode because the stripe can't be collapsed in one propagation time interval.

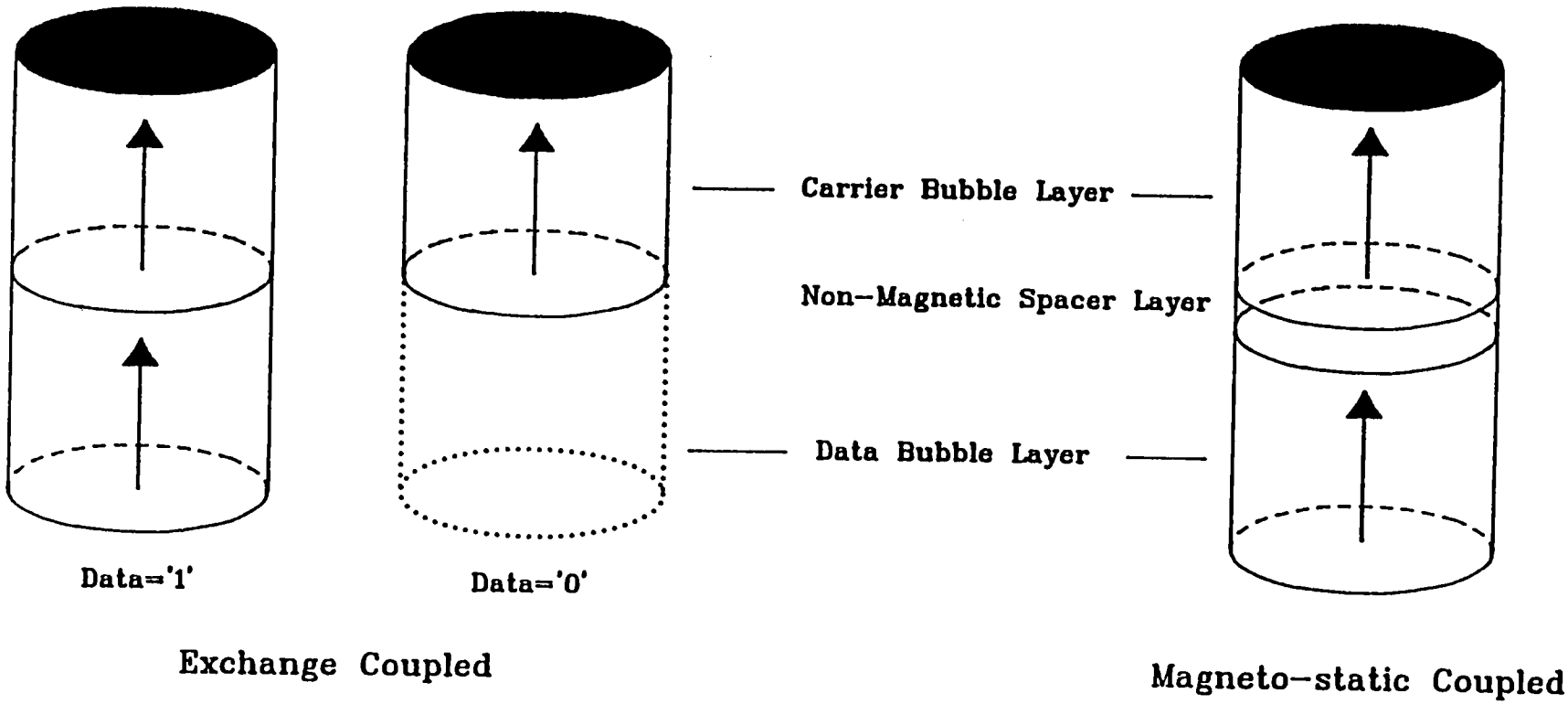
The non-stripping detection approach is desirable if sufficient signal is obtained. We observed 3.0 mV signal with this approach (see Section 3.10.3).

### 2.3.10 Data Coding

Because the self-structured approach requires a position holding bubble in every storage location, a data coding approach different than the conventional presence or not of a bubble is necessary. Two approaches, 'single/double bubble' and orthorhombic anisotropy bubble wall-state coding, are being investigated currently using Sperry IR&D funds. This work which compliments this NASA effort, will be briefly described next in order to provide a complete discussion of memory device needs. NASA contract #NAS1-15007 partially sponsored the 'single/double bubble' approach described below in previous years.

Both approaches have progressed to demonstration of the key bubble attributes necessary for the data coding problem. This includes ability to create two types of bubbles to fulfill the position holding and data coding requirements, the ability of the two bubble types to coexist at the same magnetic bias conditions, and the ability to discriminate between the bubbles for data coding. These observations were made for both approaches using garnet films grown at Sperry and using bias and relevant control fields provided by coils. No lithographic circuitry has been designed or tested as yet to make use of these bubble attributes in a test chip.

The 'single/double bubble' data coding approach uses a double magnet-layer garnet to provide for position holding and data coding needs. One layer has bubbles at all positions and can be called the carrier layer. The second layer has bubble present or not to code data and can be called the data layer. Bubbles in the carrier and data layers couple to each other so that storage locations with a bubble in both the data and carrier layers have a 'double bubble' and locations with only a carrier layer bubble have a 'single bubble' (Figure 2.3.32). This behavior has been demonstrated using magnetostatic coupling when the carrier and data garnet layers are separated by a non-magnetic layer and using exchange coupling when the data and carrier layers are not separated. The second structure is of greater interest due to less critical magnetic properties of the two layers and the elimination of the need to grow the non-magnetic layers. The 'single/double bubble' states differ essentially in the position of the capping wall which is stable on either side




Single/Double Bubble Data Coding

Figure 2.3.32

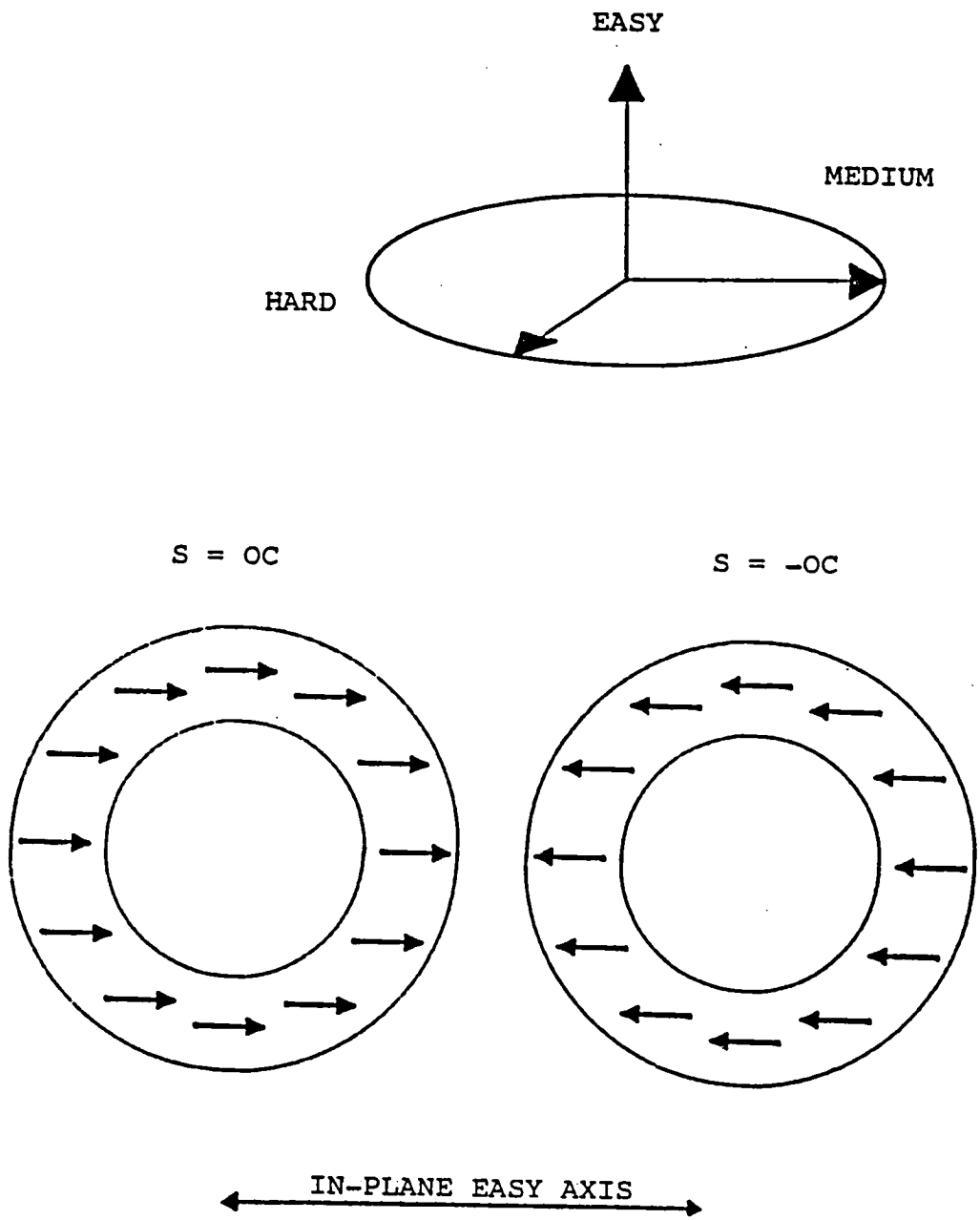
of the interface between the carrier and data layers but which must have energy applied to drive it through the interface in either direction [ 4 ]. Experimental results have demonstrated an overlapping region of bias stability for the two states, the driving of the capping wall through the interface in both directions and a difference in run out bias for discriminating the two states.

The materials required to implement this data coding research in a memory device would use (111) orientation, relatively conventional garnet bubble film compositions with fine tuning of $4\pi M$ and $H_k$ of the two layers to give the proper interface behavior. Mobilities in these typical films are such that 1.6 - 1.8 MHz data rates are possible. This satisfies the 1.5 MHz NASA specified rate.

The orthorhombic anistropy bubble wall state coding approach uses single layer, (110) orientation garnet films with compositions which have an in-plane anisotropy medium axis in addition to the usual uniaxial normal anisotropy axis. These anisotropy orientations and the data coding bubble states of interest are shown in Figure 2.3.33. Using films grown at Sperry, the ability to convert between the two circular S=0C states has been demonstrated and characterized as shown in Figure 2.3.34. In particular, note that a single |100 Oe| field pulse can result in the conversion between S=0C states without the elliptic state if desired. The elliptic bubble is another in the up to eight bubble types that have been observed in these types of films [ 5 ]. Application of lower magnitude in-plane fields than required to cause a state conversion will bias the two S=0C bubble states, one is energetically favored, the other is energetically disfavored. We have demonstrated an eight percent difference in collapse margins for the two states with this in-plane biasing as shown in Figure 2.3.35. Similar behavior holds for strip out measurements in that the energetically favored bubble state will strip out at higher bias levels than the disfavored state. Figure 2.3.35 also shows the collapse margin of the S±0C bubbles to be equal with no in-plane field. We have demonstrated that a mixture of the two states can coexist as they would be required to in a storage area.

The (110) orientation garnet materials with orthorhombic anistropy in general have much higher mobilities than conventional (111) materials and are expected to provide faster memory operation in current access propagation schemes. The material used in our experiments, BiTmYFeGa garnet has a saturation mobility of approximately 130m/sec. This gives a maximum data rate in a self-structured device of nearly 30MHz.

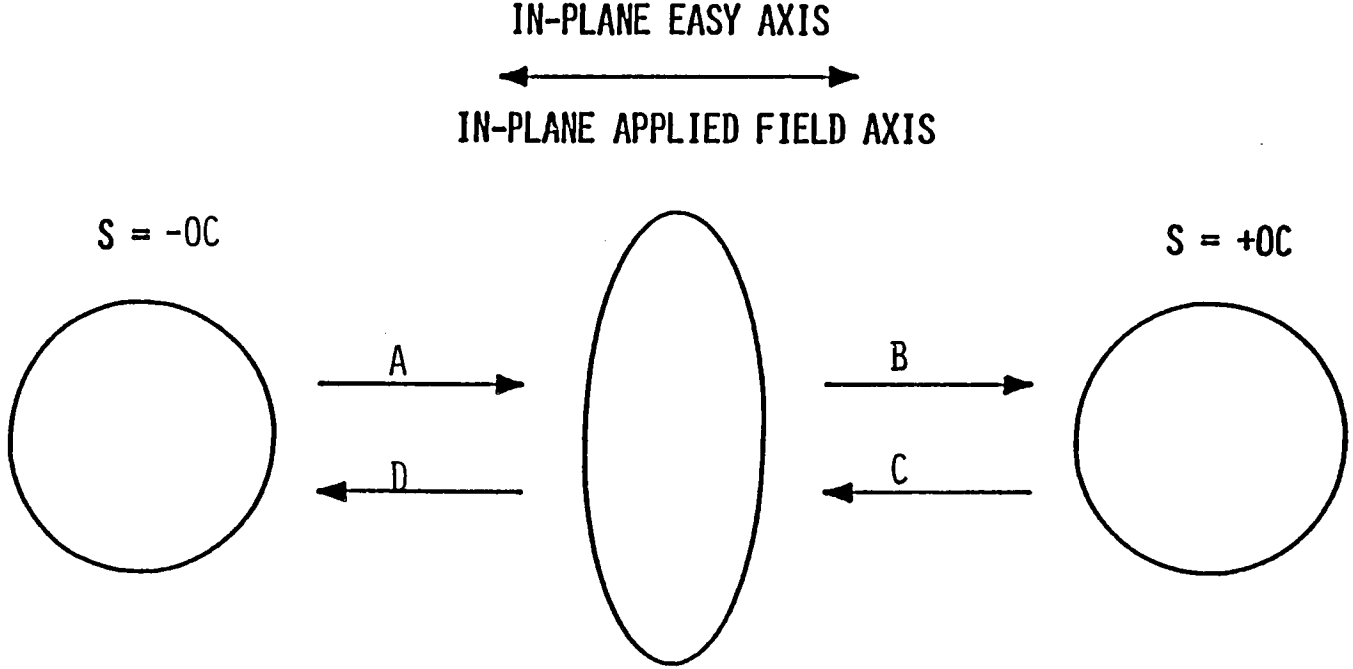
ORTHORHOMBIC ANISOTROPY:




Orthorhombic anisotropy and the wall-state data coding bubbles of interest.

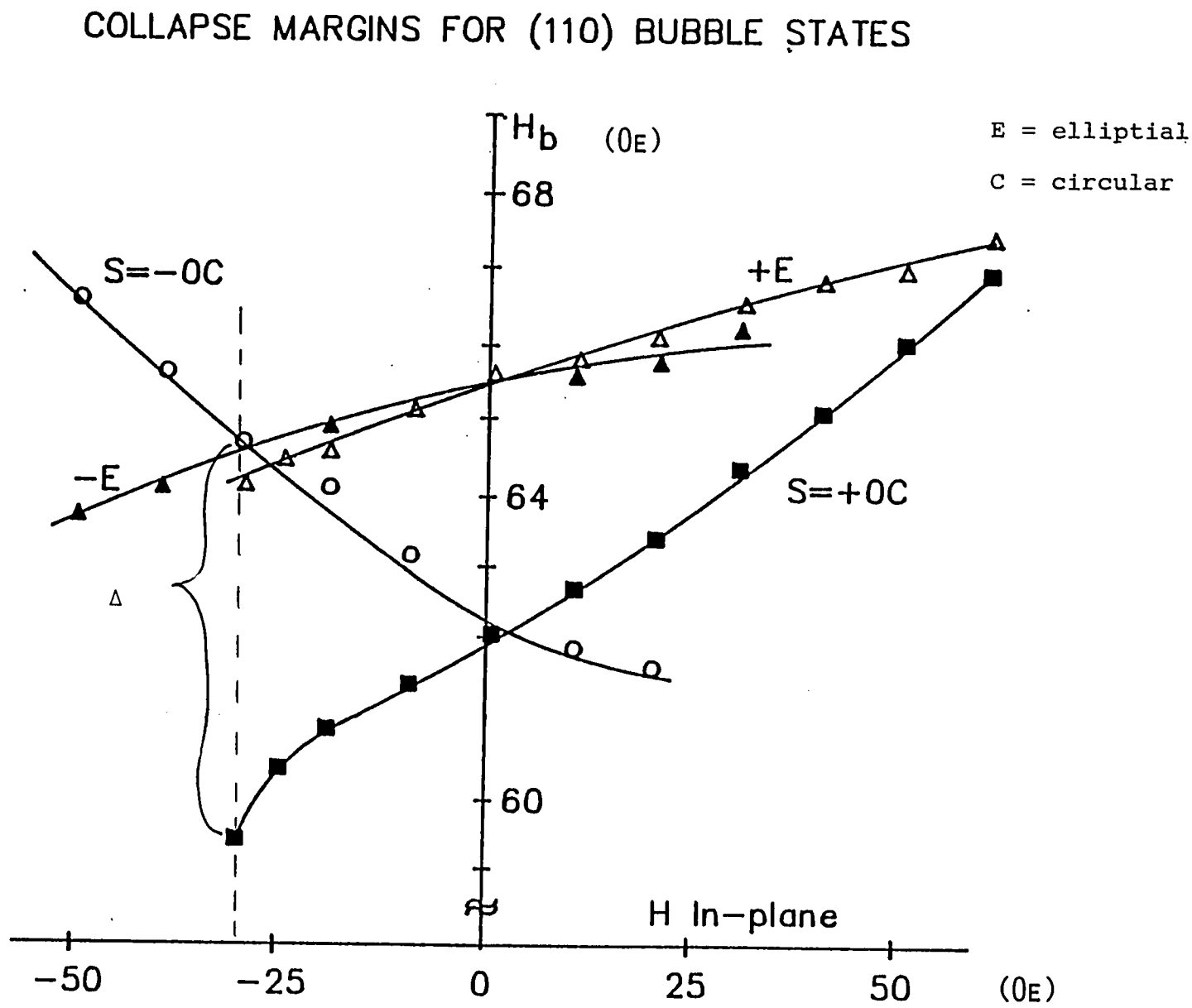
Figure 2.3.33

BUBBLE STATE CONVERSIONS IN A GARNET WITH ORTHOHOMBIC ANISOTROPY




| CONVERSION | $H_{APPLIED}$ (0E) |
|---|---|
| A | 30 |
| B | 100 |
| C | -30 |
| D | -100 |

Figure 2.3.34




Δ represents the 8% difference in normal collapse field for the S = +0C and S = 0C bubbles when an in-plane field is applied.

Figure 2.3.35

## 3.0 Experimental Component Development and Testing

### 3.1 Introduction

Based on the preliminary component set designs or needs, a series of test chips were planned. The series involved successively designing, building and testing seven chips with the goal of accumulating experimental understanding and demonstrating component feasibility as we progressed through the series.

The general question or questions addressed by each chip and the interrelationships between the chips is shown in Figure 3.1.1. There are two general approaches represented in the test chips. One is a major/minor loop type similar in philosophy to conventional bubble devices in that storage areas are rectangular and bubble columns would slip past one another as the storage area is cycled. Additionally, data I/O from the storage area to an I/O track would occur at the edge(s) of the storage area. Chips I, II, V, VI and VII address questions or components relating to this approach and some common to both approaches. The second general approach uses lattice motion of bubbles or bubbles and stripes around circular storage regions. Chips III and IV address this approach.

The details of the components and component related questions outlined in Figure 3.1.1 will be described in detail in their individual sections. Fabrication techniques will also be discussed with aspects common to all of the chips coming first (in the next section) and chip specific aspects being included in the respective sections and in Appendix A.

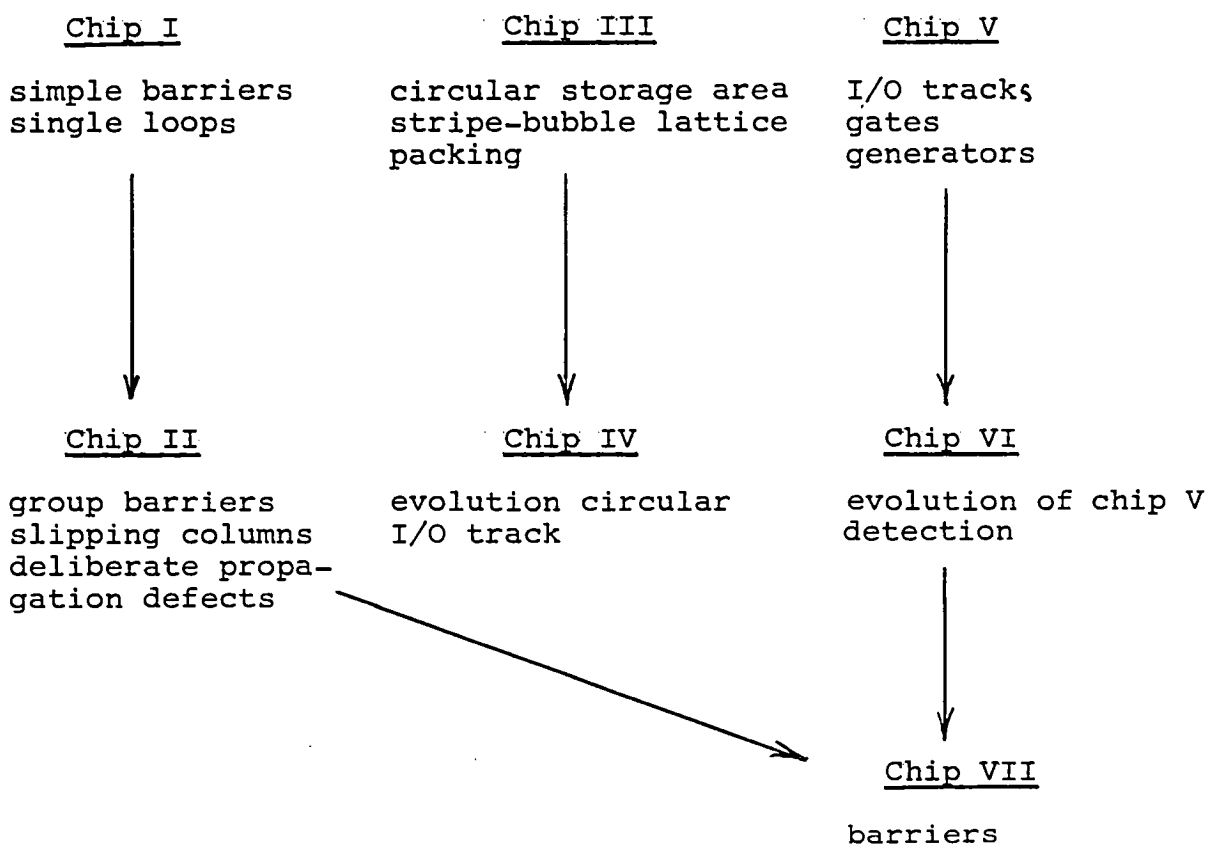
A description of the component-chip test electronics is covered in Section 3.3. In this section and elsewhere in this report, drive currents are measured in mA/μm which refers to a current per μm width of the conductor.

### 3.2 Test Vehicle Processing Overview

This section describes the materials, processes and equipment common to the processing of all test chips. These common attributes are general conductor and dielectric layers, slicing and mounting of chips, and wire bonding of circuits. Figure 3.9.3 is a generic cross section of a chip VI with two propagation conductors and a third level control conductor. It can be referenced in the following subsections.

#### 3.2.1 Conductor Layers

Conductor layers include the first and second aperture layers (drivers) and the control layer. Initially, an aluminum-copper alloy yielding 4% copper at the substrate was physical-vapor-deposited for conductor layers. The




Test chip interrelationships and component questions. Chips I, II, V, VI and VII relate to a major/minor loop style device. Chips III and IV relate to a circular lattice storage device.

Figure 3.1.1

copper additive served to prevent electro-migration and to minimize hillock growth. As the studies progressed, it became apparent that eliminating the copper did not have adverse effects on circuit fabrication and testing, and this simplification also provided better etching results when a final wet etch was used to complete the initial ion etching. It also permitted the use of a simple alkaline detergent etching solution.

Typically, the initial conductor layer was either physical-vapor-deposited or sputtered, and the other two conductor layers were sputtered exclusively in order to achieve better step coverage than would be obtainable by the normal ($90^{\circ}$) angle of incidence characteristic of the physical-vapor-deposited technique.

First and second driver layer film thicknesses were typically $\sim$3500 Å and 4000 Å respectively, while the control layer thickness was $\sim$ 4500 Å for improved ultrasonic bonding characteristics and good step coverage. A chromium overlayer 300 to 400 Å thick was physical-vapor-deposited on the two driver conductors to serve as a wet chemical etch stop while still providing an excellent adhesion layer for subsequent glass films. In instances where this chromium etch stop layer did not provide full coverage of the aluminum, rapid undercutting was noted. This would then result in either an open in the underlying aluminum driver or poor bonding to it after removal of the chromium in the vias.

Sheet resistivities of 5000 Å thick aluminum films were measured (using a 4-point probe technique) for films deposited by sputtering and by two variations of physical-vapor-deposition; RF induction and e-beam. For the particular deposition parameters used in depositing these films, the e-beam samples had the lowest value of 0.1 ohms per square. The sputtered films had a comparable value of 0.15 ohms per square, while the RF induction-deposited films had values of $\sim$0.3 to 0.4 ohms per square. Films deposited by the latter technique typically had a brownish color on the upper surface, possibly indicative of contamination, while the bottom surface (as seen looking through a glass test substrate) was typically very silvery and reflective in appearance. Outgassing of film layers on the inside of a chimney assembly located above the vapor source is believed to be at least partially responsible for this phenomenon. These findings, along with the fact that the sputtered films afforded better step coverage, led to the selection of sputtering as the preferred deposition means for the conductor layers.

An extensive comparison study of roughness of aluminum films sputtered under various conditions was conducted using a scanning electron microscope (SEM). These films were approximately 3000 Å thick, and all were deposited on glassy, smooth surfaces (either glass or thermally oxidized silicon) after an initial 2 to 5-minute sputter etch cleaning of the substrate. High deposition rates ($\sim$6000 Å/min.), typical for a bipolar metallization process used at Sperry, were achieved using an MRC 603 D.C. sputtering system operating at 8 KW in an atmoshpere of 9 µm of argon. Lower rates ($\sim$600 Å/min.) were also evaluated, using 2 KW D.C. power. Of the high deposition rate films, the smoothest were those that had no bias voltage applied to the substrate electrode and no supplemental heating. For the lower deposition rate films, a 125 V. bias gave a smoother film surface than when no bias was applied. Neither of these latter films had supplemental heating. These studies provided helpful guidelines with regard to deposition rate, bias and supplemental heating.

An RF sputtering system with a 5" x 12" Vac-Tec magnetron-type cathode was used to deposit most of the aluminum films for the bubble circuits. The smoothest films were obtained when no supplemental heating or bias were used during deposition and when the vacuum system was pre-baked for 7 hours at $\sim$100°C, followed by a 2-hour cooldown. This procedure provided a base pressure of $\sim 8 \times 10^{-7}$ Torr in a diffusion-pumped, liquid nitrogen-trapped system. Using an argon plasma, the sputtering pressure was controlled at $\sim 8 \times 10^{-5}$ Torr. Deposition rate was $\sim$200 Å/min. based on profilometer thickness measurements made on a Dek-Tak II instrument. Thickness was controlled by power and deposition time.

Bubble circuits were lightly back-sputtered prior to aluminum deposition to remove any surface contamination that might affect adhesion or cause increased interface resistance between contacting layers such as the NiFe detector elements and the aluminum control conductor.

### 3.2.2 Separation/Insulator Layers

SiO

A 3000 Å thick SiO separation (spacer) layer was initially deposited directly on the garnet surface, prior to the first driver conductor layer, to provide a geometry more conducive to equal drive influence on bubbles from the two driver conductors. This layer was physical-vapor-deposited (sublimed) from a molybdenum crucible using R.F. induction heating. Substrate temperature was nominally 100°C.

Adhesion of SiO to the garnet surface was good and, in turn, aluminum adhered well to it. This layer also served to prevent damage to the garnet surface in the event of overetching of subsequent layers.

Polyimide

As potential advantages of polyimide organic film became more apparent, the spacer layer in later circuits was switched to members of this family of materials, [13]. The polyimide film served the same purpose as the SiO, and it also provided a conformal, near-planarizing effect on barrier steps (when present) which is important to good step coverage by subsequent film layers. Planarization with polyimide is typically good because the films are dispensed as liquids and spincoated prior to curing.

Polyimide films also appear to make ideal interlayer dielectrics because of their high dielectric strength, ($1.57 \times 10^6$ v/cm) low defect density, ease of etching and controllable via profiles [6]. The dielectric constant is a low 3.5.

Because the use of polyimide as a dielectric layer between drivers and between control conductor and driver was not used extensively in the bubble circuit fabrication studies, the glass used most for this purpose is described next. More is said about polyimide, its advantages, problems and processing in Appendix A.

Glass

The glass dielectric used [14] is a barium aluminum borosilicate composition which is alkali-free and characterized electronically by a very high volume resistivity ($10^{13}$.1 ohm-cm at 250°C), a dielectric strength of $1.17 \times 10^6$ v/cm and a dielectric constant of 5.9 at 1 MHz.

Its use as an insulating layer between driver conductors and between control and driver conductor was also predicated on its adhesion compatibility with SiO, polyimide, chromium and aluminum, its low defect density and its ease of etching to form vias (using $13NH_4F$:1HF).

The glass films were RF sputter-deposited in a diffusion-pumped, liquid nitrogen-trapped vacuum system similar to that used for sputtering aluminum layers. The target was bonded to a 6½" round magnetron cathode. Background pressure was typically $5 \times 10^{-7}$ Torr prior to introduction of argon to a pressure of 7 μm. For each deposition, a pre-sputter target cleaning step and a reverse-sputter substrate cleaning step were performed. Thickness was typically 9,000 - 10,000 A, and no supplemental heating was used.

When utilizing polyimide as the spacer layer, a capping layer of 7059 glass was sputtered over the polyimide to nominally seal the surface from water absorption and prevent outgassing during subsequent film depositions. This also tended to lend rigidity to the polyimide and prevent outgassing during wire bonding, resulting in better bond adhesion. The 7059 thickness in this case was 2,000 Å.

### 3.2.3 Chip Slicing/Mounting/Bonding

The original garnet crystals were in the form of 3" diameter wafers. These were scribe-cut on a Rucker & Kolls Model 400 wafer dicer/scriber saw with diamond cutting wheel and broken into 3/4" square pieces. Film deposition, photolithography and processing were then conducted on these pieces, each of which had 3 or 4 circuit patterns on it.

Prior to dicing into individual chip circuits, these crystals were bonded to a silicon wafer using a thermoplastic (Crystal-Bond) and were then spin-coated with Shipley's photo-resist for protection. The same diamond saw was then used to cut completely through the crystal, forming individual dies. The photo-resist was then removed with acetone, followed by heating on a hot plate to melt the thermoplastic. After removing the dies (chips) the thermoplastic was removed in an ultrasonic acetone bath and spray rinse.

Each chip was bonded to its own gold-plated P.C. "paddle" board using small dots of Crystal-Bond at four points around the periphery of a hole in the board (used for Faraday magneto-optic observation of bubble behavior). This "paddle" matches microscope test stations both at Sperry and at NASA-Langley.

Wire bonding from the circuit board pads to the chip pads was accomplished with 0.001" diameter aluminum wire using a Kulicke & Soffa Model 4123 ultrasonic wedge bonder.

### 3.2.4 Garnet Materials

All test circuits were fabricated on $Y_{1.92}Sm_{0.1}Ca_{0.98}Fe_{4.02}Ge_{0.98}O_{12}$ films with nominal thickness, h of 6.0 μm, magnetization, $4\pi M$ of 130G, and uniaxial anisotropy, $H_K$ of 670 Oe. These properties give a near-strip-out bubble diameter of 5.5 - 6.0 μm.

## 3.3 Bubble Component-Chip Test Electronics

A bubble tester system was constructed as part of the contract. The design goals were to provide a testing capability with a propagation frequency range from psuedo dc for microscope observations to 100 - 200 KHz for gate and/or high speed operation. Most importantly, the pulse

sequence, width, delay and amplitude must be programmable during a high speed burst to accommodate gate testing, besides being reprogrammable between bursts.

The general outline of the tester is shown in Figure 3.3.1. The system has a number of pulse generators which are pre-programmed to specific pulse characteristics. The direct memory access (DMA) controller then outputs preprogrammed sequence control data from RAM through the general purpose input/output (GPIO) interface to trigger (select) a particular pulse and route it to the appropriate power driver. Sixteen data lines are available for trigger control of external generators. The rate of output from the GPIO interface is controlled by handshaking with an HP 8116A function generator and can range from a minimum frequency of less than 1 hertz to a maximum of 750 - 1000 KHz. With this approach, a given test device line can be driven at up to a megahertz frequency with preprogrammed pulse to pulse phase, amplitude, and width control. This provides the flexibility in high speed, over-lapping (device line vs device line) testing required, for example, by bubble replicator gates. The ratio of the GPIO output sequence control data rate, and the propagation rate determines the resolution within a propagation interval for control conductor timing or propagation pulse timing variation.

The bipolar power stage has two different implementations presently. One uses power MOSFETS, the other uses integrated circuit memory drivers.

Figure 3.3.2 shows the MOSFET circuit. The test device is driven by the differential voltage developed when either of the nominally off MOSFETS is turned on in an analog fashion. The benefits of this power stage are its high speed (5 nSec switching), high current capability (>1 amp), and ability to easily mix drive pulses of unequal pulse amplitudes. The disadvantage is that the test device is normally floating at 40 volts. This has caused problems when a lead to the test device is accidently grounded placing 40 volts across the device which destroys it. The 40 volts also caused problems when third level control conductors, driven by pulse generators nominally holding, for example, a gate conductor at zero volts, effectively put 40 volts across the dielectric layer resulting in breakdown and at least damaging a region of the test device. Multiple analog control inputs can be "OR"ed to either input to permit mixing pulses of different timing, amplitude, polarity and width to a test device's lead. With the DMA data dumping, pulse mix can be preprogrammed so that bursts of almost any pulse mix can be provided.

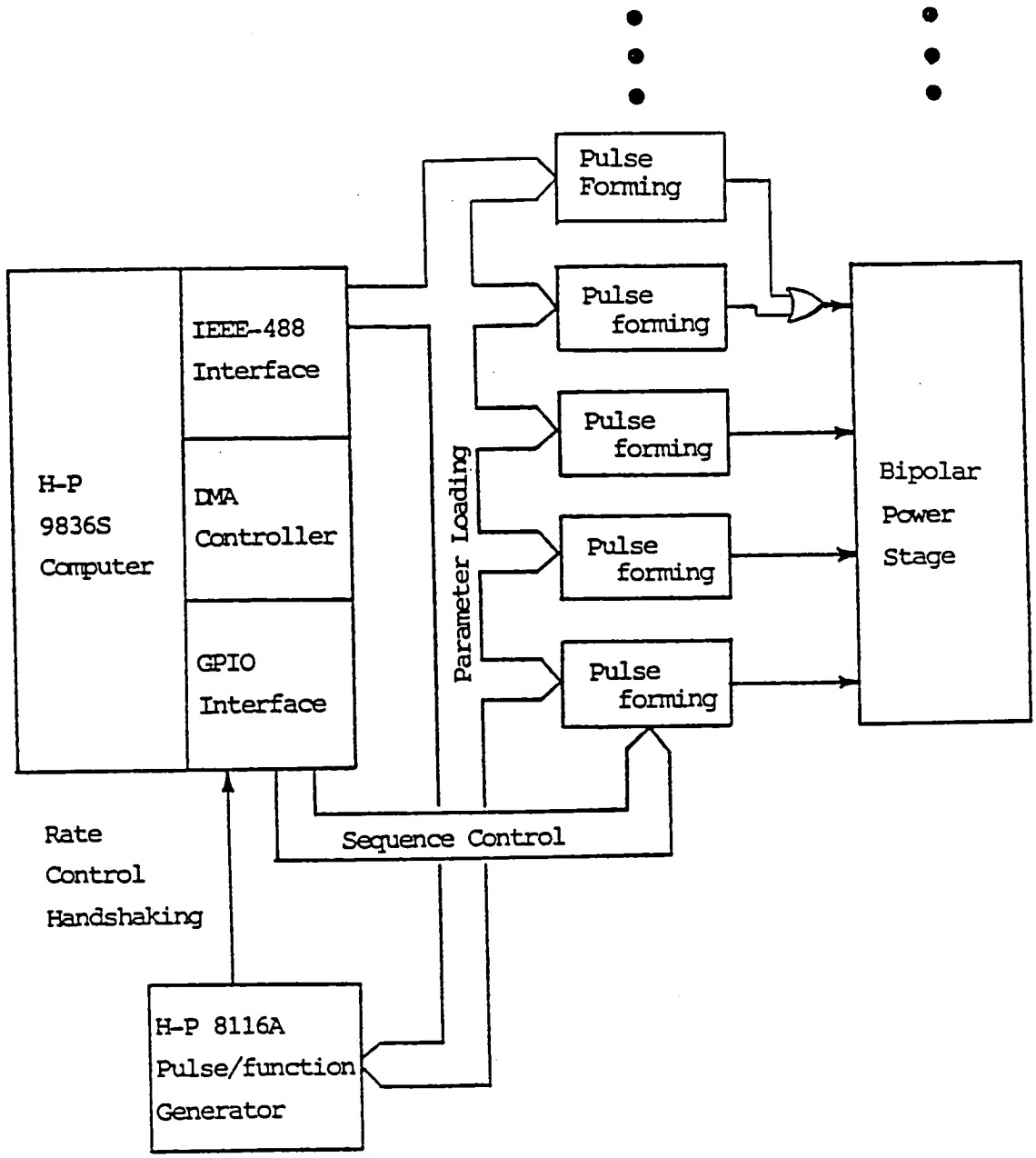



Figure 3.3.1 Bubble Circuit Tester Based on Hewlett Packard 9836S.

Figure 3.3.2 A power MOSFET driver provided high speed, large current pulses (as described in text) but kept test device floating at 40V.

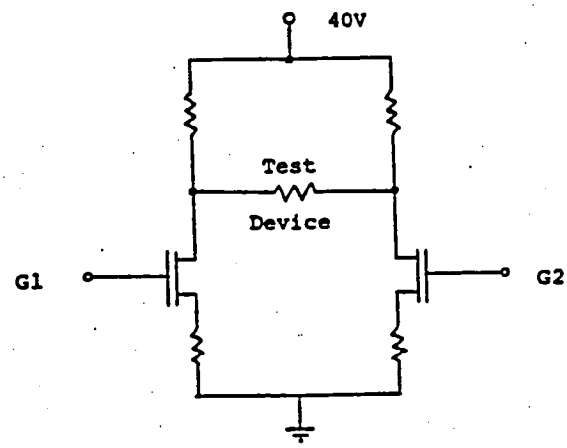



Figure 3.3.3 Bipolar memory driver IC's were limited in speed and current capabilities compared to the 3.3.2 driver; but test device is nominally kept at ground potential.

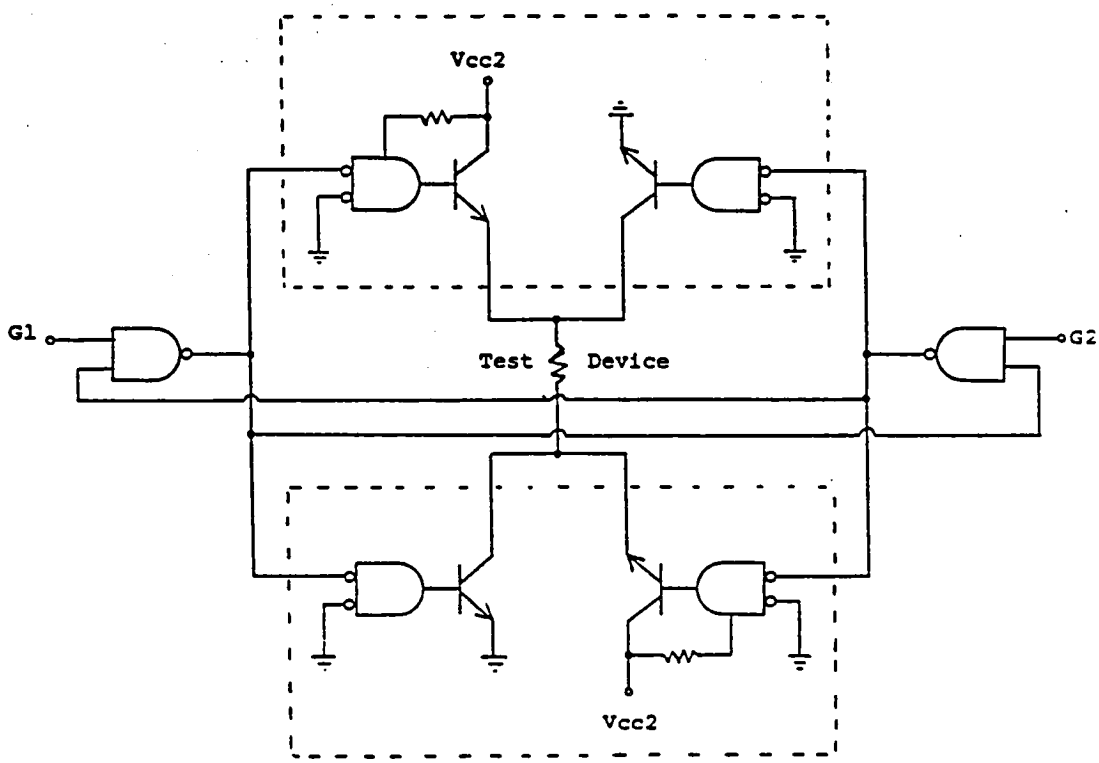


Figure 3.3.3 shows the bipolar integrated circuit power stage. It uses low cost integrated circuit memory drivers. These I.C.'s consist of TTL logic selectable current sources and sinks which can handle 600 - 750 mA of current. This provides a maximum of 1.2 - 1.5 mA/μm current levels in present bubble test chips and is perfectly matched to the 0.75 - 1.5 mA/μm levels tvpically used in testing. If more current is needed, the memory drivers can be paralleled to meet any foreseeable current needs. By appropriately selecting the source-sink polarity across the bubble test chip conductor, the desired current direction can be chosen. The driver as shown in Figure 3.3.3 simply takes a TTL level gating pulse (G1 or G2) to produce the desired polarity of current flow. Amplitude of the current pulse is controlled by Vcc2. The NAND gates used at inputs G1 and G2 simply prevent both source-sink pairs from being turned on simultaneously.

The advantage of this power stage compared to the MOSFET stage is that the test device is nominally at ground potential and that TTL inputs are used for control. The disadvantages are slower speed (50nSec switching), lower maximum current for non-paralleled driver circuits, and greater difficulty implementing computer controlled, unequal pulse amplitudes. For this power stage, simple TTL inputs can be "OR"ed to mix pulses with different widths but the sacrifice is the amplitude control.

## 3.4 Chip I - Barriers and Simple Storage Loops

### 3.4.1 Chip I Description:

Chip I is an apertured dual conductor bubble propagation circuit, which has eleven different propagation loops which are repeated in four groups with variations. Each loop has a different design of a bubble barrier, where the object of the barrier is to preserve the natural bubble lattice spacing that has been designed into the propagation apertures. As the bubbles propagate around these simple loops, bubbles on one side of the loop are propagating in a direction opposite to those on the other side of the loop. Since the rows of propagation apertures have been placed closer together then in non-self-structured devices, the loop propagation results in two rows of bubbles slipping past each other and being pushed against the barriers due to bubble to bubble repulsion. A simple closed loop of propagating bubbles, with a method of confining these closely packed bubbles, is a basic building block of the major/minor loop memory design.

Figure 3.4.1 illustrates a portion of Chip I, showing some of the eleven propagation loops and barriers. The barriers were created by ion-milling the garnet, removing from 0.2 to 0.8μ from the garnet which is approximately 7.0μm thick. As a result of the ion-milling, the resulting barriers include mesas, channels, craters and recesses where recesses are wide channels entirely containing the storage loop.

Figure 3.4.2 displays the photomask used for defining the barriers. The dark areas are regions where the garnet surface was ion-milled. Ten barrier types are illustrated in the figure, and one of the eleven propagation loops has no garnet barrier. The loops and barriers are described as follows:

1) "real bubble" barrier

2) "crater" barrier

3) "sinusoidal narrow channel"

4) "variable spacing and width channel"

5) "narrow, straight channel"

6) "narrow, sinusoidal mesa"

7) "narrow, straight mesa"

8) "wide, straight mesa"

9) "sinusoidal recess"

10) "straight, narrow recess"

11) "straight, wide recess"

Propagation loops in Figure 3.4.1 and barriers in Figure 3.4.2 are labeled with the above identification numbers. They will be described in more detail next.

The 'real bubble' barrier (1) is basically a control loop having no ion-milled structure. The loop also, however, provided the first experimental opportunity to observe bubbles being propagated while surrounded by interacting bubbles.

The 'crater bubble' (2) allows essentially simmulating bubbles which are fixed in position. Placement of these craters, milled into the garnet surface, can take the form of a hexagonal structure, and can assist in defining the

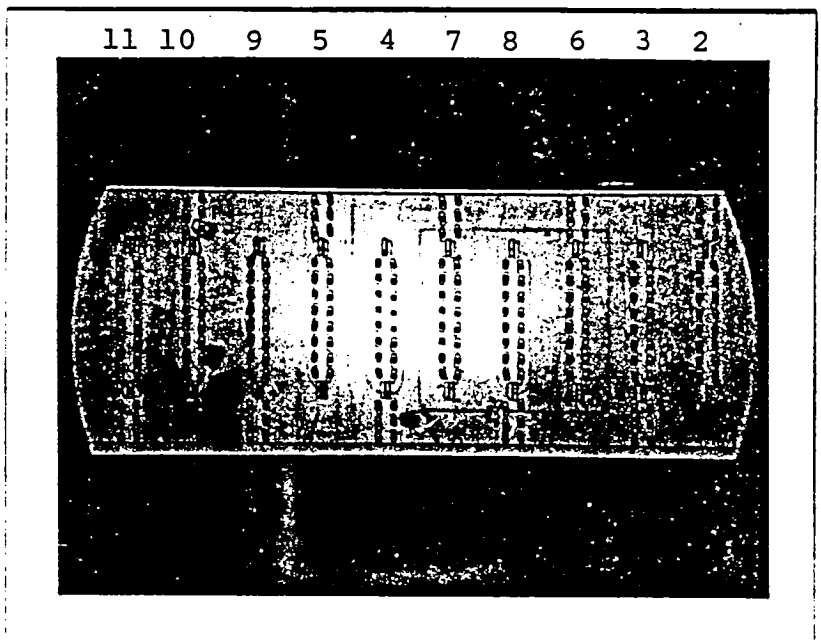
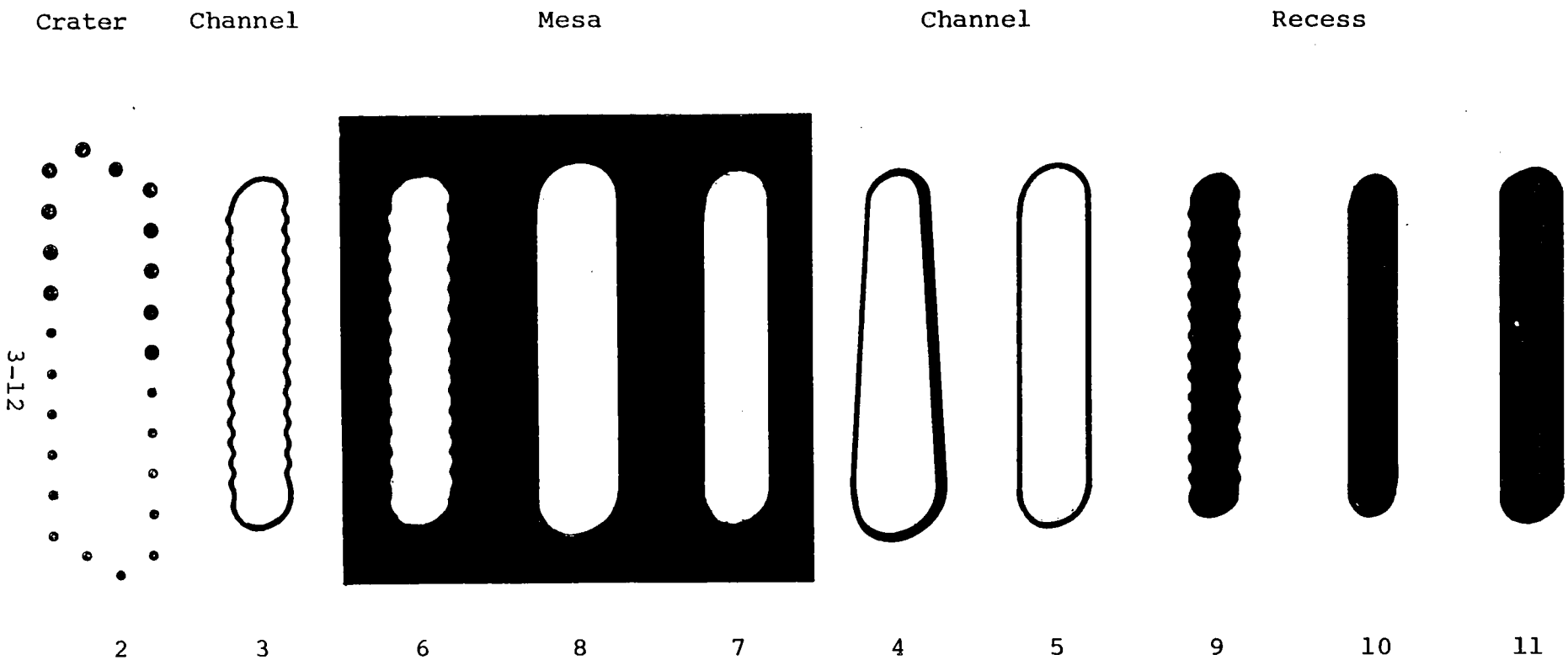



Photo of a chip I sample showing propagation loops and barriers.

Figure 3.4.1




Barrier pattern for Chip I

Figure 3.4.2

bubble lattice structure. Additional rows of craters could be included for additional barrier control. If the craters were milled completely through the garnet, this void would appear to a bubble as a neighboring bubble with one-half the magnetization of the garnet.

Channel barriers (3,4,5) are milled channels of approximately a bubble diameter in width which are placed around the loop at various spacings and with various widths. This structure effectively simulates a stripe domain, with reduced magnetization, as the barrier.

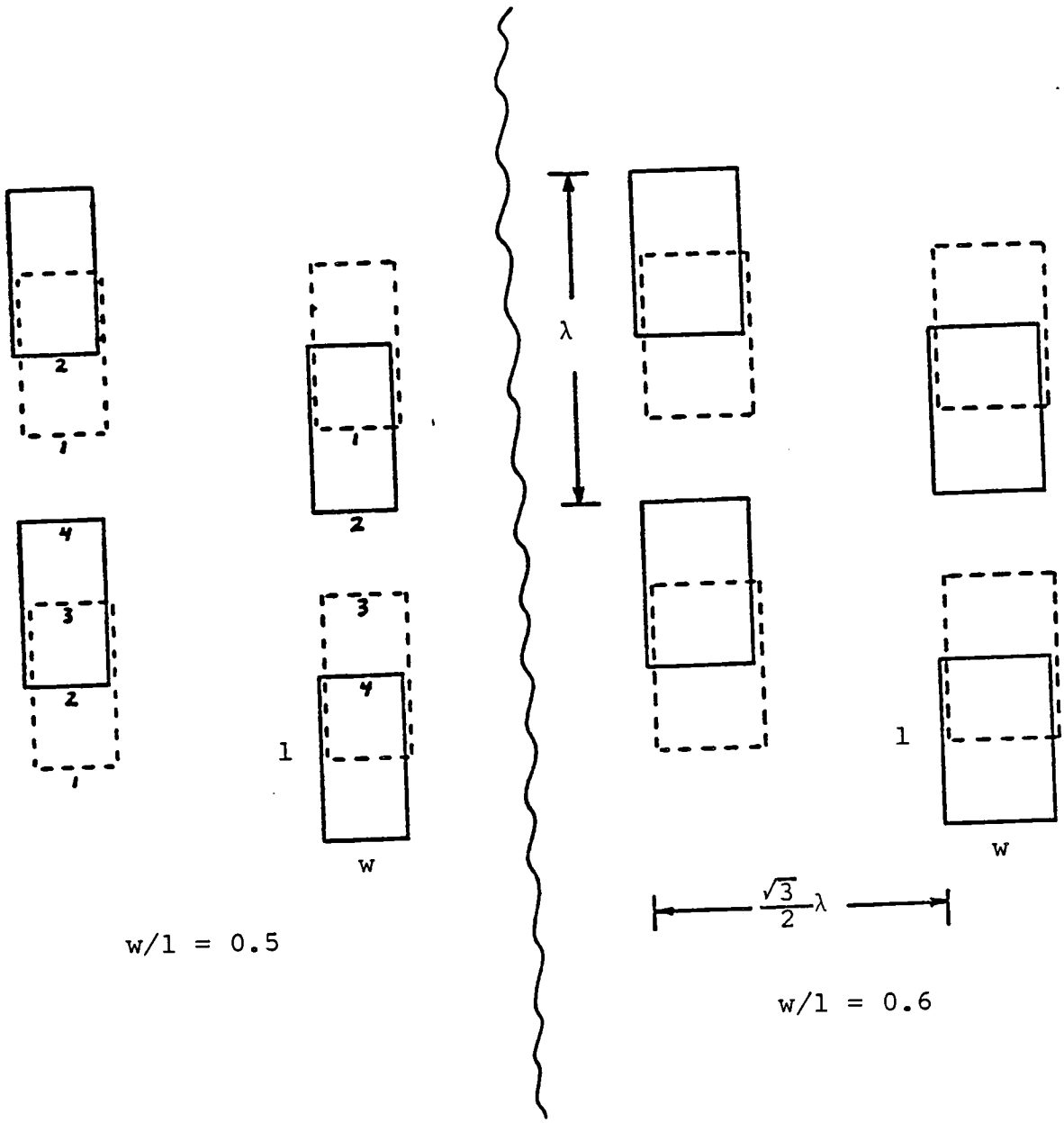
Mesa loops (6,7,8) have the entire propagation loop on a raised mesa region formed by milling away the surrounding garnet. Bubbles are repelled by the mesa edge again as from a domain with the same magnetization sense although with a lower magnitude.

Recess loops (9,10,11) place the storage loop inside the milled region, essentially a reversal of the mesa structure. In this case bubbles are attracted to the milled (loop) side of the thickness discontinuity.

The sinusoidal shape of some of the barriers allows a more uniform force (spacing) between bubbles as they're slipping past one another in the two columns. This shape also lends position stability to the bubble lattice when it is alternately switched between hexagonal and square packing during propagation.

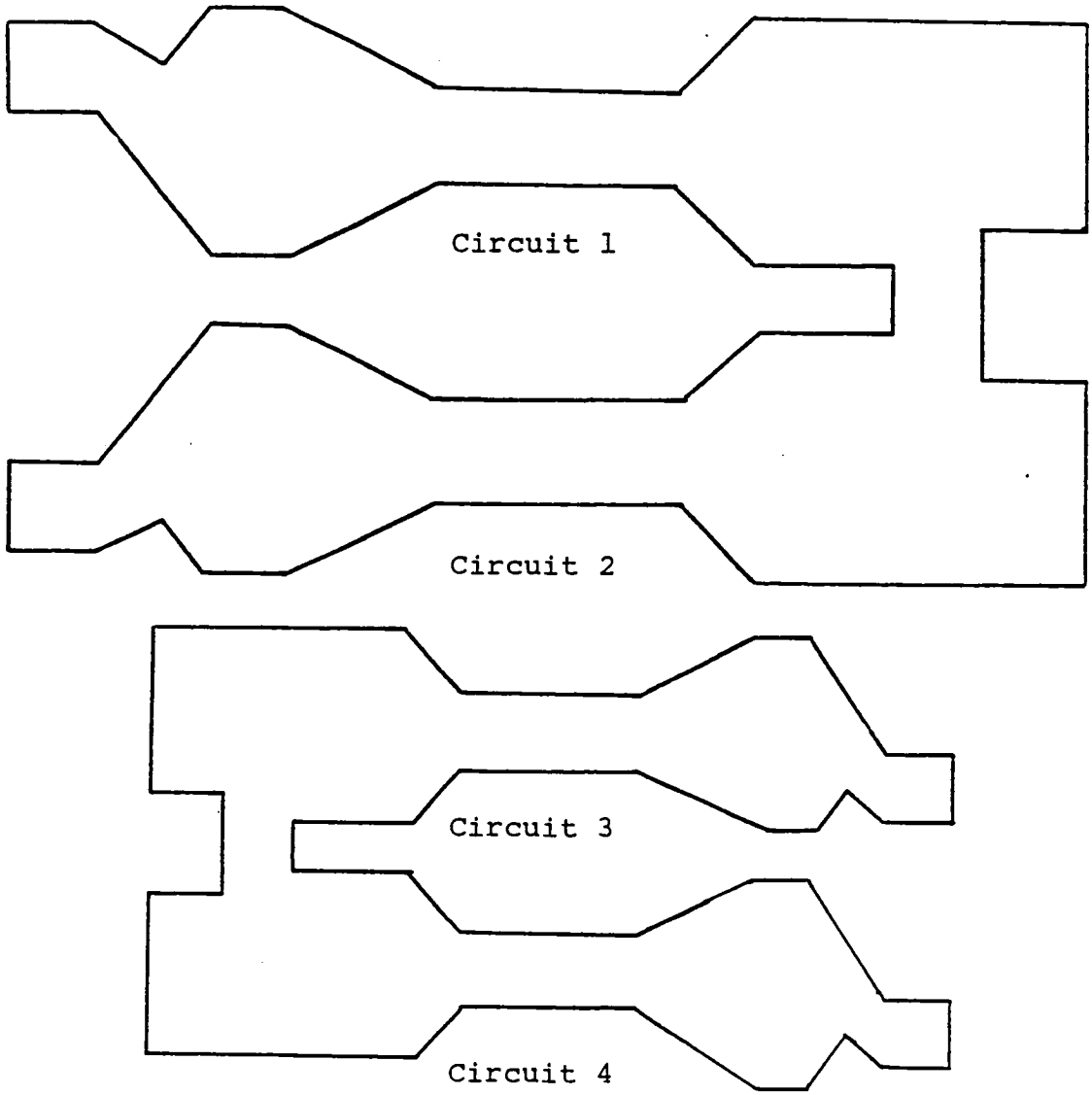
The four groups of these eleven loops vary the aspect ratio of the propagation apertures and vary the overall scale of the storage loops relative to bubble diameter. Figure 3.4.3 shows the two aperture shapes used. One shape uses width/length of 0.50. The other used width/length of 0.67. In general, testing was performed using the 0.67 aspect ratio apertures. These two shapes are used to make two of the four groups. The remaining two groups are a repeat but at a 0.75 scale factor. The complete Chip I conductor outline for one of the propagation conductors is shown in Figure 3.4.4. The two loop scales allow a wider range of bubble spacing ($\lambda$) to bubble diameter (d) to be explored than can be achieved with bias field changes alone. For the material used and the circuits built, the $\lambda/d$ for the larger loops can be varied with bias field from 3.5 to 4.5. For the smaller side loops, $\lambda/d$ ranges from 2.5 to 3.5.

The overall dimension of Chip I is 0.25 inch by 0.25 inch, and the "active area" of each of the two large test circuits is approximately 400 μm by 800 μm. The 75% reduction for the two smaller circuits gives an "active area" near 300 μm by 600 μm. Only 60% of the conductor width is used for the




Propagation apertures.

Figure 3.4.3




Test circuit conductors for Chip I.

Figure 3.4.4

propagation loops in order not to subject the bubbles to the large normal magnetic field generated by the conductor near its edge. Neighboring sides of a loop are separated by four propagation steps or 1 λ.

### 3.4.2 Chip I Planar Fabrication Using a Polyimide Dielectric Spacer:

A polyimide spacer was used successfully to cover the ion machining of the garnet and provide a planar surface for subsequent fabrication layers. A number of interesting things were learned about using polyimide in this type of an application. Profiled barrier steps where the ion machining process was tailored to give more gradual garnet thickness changes were also developed for fabricating devices without polyimide. Both of these topics are covered in Appendix A - Fabricating Circuitry Over Ion-machined Garnet Barrier Steps.

### 3.4.3 Chip I Testing Results:

Chip I testing results are presented in terms of:

- General observations near midpoint bias and propagation current densities,
- Bubble propagation as a function of propagation current with fixed bias field, and
- Bubble propagation as a function of bias field with fixed propagation current.

These observations were all made using the second circuit in Figure 3.4.4 which is the large scale circuit with apertures of 0.6 aspect ratio. Propagation on the smaller circuit, number three in Figure 3.4.4 is described subsequently, followed by a summary or conclusion about the relative performance of the different barriers.

Chip I Relative Barrier Behavior:

The following components describe the propagation of bubbles at a conductor current density of 0.5mA/μm with 5μs wide non-overlapping bipolar pulses. The normal bias field is approximately 48 Oe. The milling depth or barrier step height is 0.2μm with a sharp step and polyimide planar base for the propagation conductors. Testing speeds were psuedo DC so that observations of bubble behavior could be made.

1. "Real Bubble"

This propagation loop requires neighboring bubbles in the lattice to provide the barrier action required to maintain the proper bubble location around the loop. The loop works well if fully populated but is subject to bubbles comprising the 'barrier' and the loop swapping positions when the loop is not fully populated.

2. "Craters"

These small regions milled into the garnet provide a barrier behavior similar to a bubble at the same location, but with a reduced effect. At this milling depth (3% of h), the craters were too weak to improve much over the control loop #1. However, many of the craters captured bubbles that were outside the propagation loop. The loop works well with these captured bubbles in the barrier craters. A combination of deeper milling and captured bubbles could be a good, stable barrier. The benefits include 2-dimensional positioning control and the possibility of ignoring conductor continuity over the 'barrier' since only $\sim$25% of the conductor crosses a step.

3. "Sinusoidal, Narrow Channel"

Bubbles outside the loop are attracted to the outside of the inner channel edge, resulting in these bubbles being too close to the propagation apertures and bubbles in the loop. When several outside bubbles are present on both sides of the loop, bubbles in the loop will move into the central region of the loops and will not propagate. However, the loops works well if there are no bubbles on the outside of the channel in that the loop bubbles are effectively contained.

4. "Variable Spacing and Width Channel"

As the bubbles propagate around the loop towards the narrow end of the barrier loop, many of the bubbles jump into the wide part of the channel ($\sim$ 1 d wide) and remain in this location blocking further propagation at this end. At the other end of the loops, where the channel is further away from the apertures, bubbles circulate properly, albeit in a shortened loop due to the blocking at the other end. At higher propagation current levels, greater than 1.0 ma/μm, where the magnetic fields from the apertures can move the bubbles in the channel, the whole loop would function with bubbles jumping in and out of the channel as energetically expedient.

5. "Narrow, Straight Channel"

Bubbles in the loop attach to the inside of the outer step of the channel, thereby placing themselves too far from the apertures for proper propagation. This is similar to the behavior of the out-of-loop bubbles in #3 above.

In both cases, bubbles want to occupy the channel. Being approximately 1/2 d in width, the channel doesn't do this well either and results in generally unstable operation at its best.

6. "Narrow, Sinusoidal Mesa"

The edge of the mesa barrier is too close to the apertures in the propagation track. This results in the outside bubbles, which are attached to the barrier, forcing the active bubbles into the center of the loop. Barrier behavior in terms of bubbles crossing in or out was good.

7. "Narrow, Straight Mesa"

This barrier behaves the same as number 6.

8. "Wide, Straight Mesa"

Outside bubbles are again attached to the edge of the mesa, but in this design the spacing between these attached bubbles and those in the storage loop columns is close to the natural lattice spacing, which allows both the mesa edge positions and the propagation track positions to be occupied by bubbles. This loop works well.

9. "Sinusoidal Recess"

Bubbles in the propagation track are nicely attracted to the edge of the recess barrier, which is positioned quite close to the apertures. This design thereby places the bubbles perfectly for the apertures. Bubbles follow the sinusoidal edge of the barrier during propagation, demonstrating that this design works well.

10. "Straight, Narrow Recess"

This design works well, similar to number 9, at low conductor current densities. At high current densities, active bubbles are sometimes ejected at the ends of the loop, and many bubbles center themselves along the barrier edge.

11. "Straight, Wide Recess"

Bubbles in the loop are atracted toward the barrier edge, the same behavior as loops 9 and 10. Because of the extra width of the recess, however, the bubbles are moved away from the propagation apertures. With or without bubbles outside the barrier, active bubbles propagate well. Due to the wide recess, the propagation looks sloppy, but it works.

Propagation Current Behavior:

Observation of bubble propagation in circuit number 9, sinusoidal recess, and number 10, narrow recess barrier, as a function of the bipolar conductor current magnitude are presented in the following table. A current pulse width of 5μs, and a normal bias field of 49 oe were employed for these tests. At this bias field, bubble spacings are approximately 3.5 bubble diameters.

| Conductor Current | Circuit #9 | Circuit #10 |
|---|---|---|
| ma/μ | | |
| 0.25 | Bubbles moving slightly. | Bubbles moving slightly. |
| 0.38 | Bubbles are moving, but having problems when not aided by lattice but opposed by counter direction bubbles. | Bubbles propagating fairly well. |
| 0.50 | Good propagation. | Good propagation. |
| 0.75 | Good propagation, but one corner temporarily strips out bubbles as they pass. | Good propagation. |
| 1.0 | Bubble stripping at ends of loop with occassional bubble rejection; some tendency for bubbles to move to outside of barrier. | Same as #9. |
| 1.5 | Same comments as for 1 mA/μm, except the effects are more pronounced, bubbles stripping at the middle of the loops. | Same as #9. |

Based on the results presented above, loop #9, sinusoidal recess barrier, was tested for bubble propagation with a fixed conductor current as a function of the normal bias field. The conductor current density was 0.60ma/μm. At this current density, the data below demonstrates an average bias field operating margin of 20%.

| Bias Field (Oe) | Performance on Circuit #9, Sinusoidal Recess Barrier | $\frac{\lambda}{d} = \frac{\text{period}}{\text{bubble dia}}$ |
|---|---|---|
| 41.3 | Some bubbles strip out. | |
| 44.6 | Bubble diameter approx. 110% of aperture width; some bubbles strip out. | 3.0 |
| 47.0 | Bubble diameter approx. equal to aperture width; some bubbles punch through the barrier, but are not lost. | 3.3 |
| 49.4 | Bubble diameter approx. 85% of aperture width; bubbles propagate smoothly along track and place themselves nicely in the sinusoidal barrier wells; bubbles do not hang on or jump through the barrier. | 3.9 |
| 50.5 | Bubble diameter 80%; works well. | 4.2 |
| 53.5 | Bubble diameter 75%, works well. | 4.4 |
| 54.7 | Bubble diameter 66%, works well. | 5.0 |
| 59.5 | Bubble diameter 50%, works well. | 6.7 |
| 60.6 | Bubble diameter 40%, most bubbles have collapsed. | 8.3 |

Propagation of Tightly Packed Bubbles in Circuit #3(Figure 3.4.4)

Propagation with smaller bubble-spacing to bubble diameter ratios has also been demonstrated using Chip I. This was done using the 'smaller scale' half of Chip I which provides

a spacing to diameter ratio of 2.5. This is an important result in that a ratio of 2.5 - 3 is necessary for a $10^7$ bit chip using $\sim$2 micron bubbles. Margins have not been accurately measured but in general, the propagation currents need to be higher (1.5mA/micron) due to the smaller size of the apertures in the propagation conductors.

Conclusions About Barriers:

1. The shallow barriers used in these tests cannot generate the forces necessary to arbitrarily position the bubbles without regard to the nominal lattice spacing.

2. Large current pulse amplitudes in the conductors expand the bubbles enough, so that if the garnet barrier is nearby, the bubble will penetrate the barrier and thereby be susceptible to being ejected from the loop.

3. Narrow channels tend to mix bubbles from both sides of the channel.

4. Two dimensional positioning abilities of the craters and the sinusoidal barriers aid the placement of the bubbles and promote smooth propagation under proper conditions of bias field, conductor current, and barrier spacing.

5. The recess barrier appears to offer the best control and confinement of all the barriers tested and evaluated. Its weakness is the proximity of the barrier and the ejection of bubbles at high propagation currents with low bias fields. However, the barrier works well at the desired low propagation currents. Because the active bubbles are exactly positioned by the barrier, optimum interaction with the apertures can be obtained. Since the barrier presents a repulsive force to bubbles outside the loop, these bubbles are not affected by the propagation fields, and the contamination effects are reduced.

6. No conclusions were formed about the 0.5 aspect ratio apertures versus 0.6 aspect ratio apertures. Most testing, however, used the 0.6 aspect ratio apertures as they more closely approximate the aperture shape expected in a device using $\sim$2μM diameter bubbles (aspect ratio of 0.8).

## 3.5 Chip II - Group Barriers, Slipping Bubble Columns and Deliberate Propagation Defects

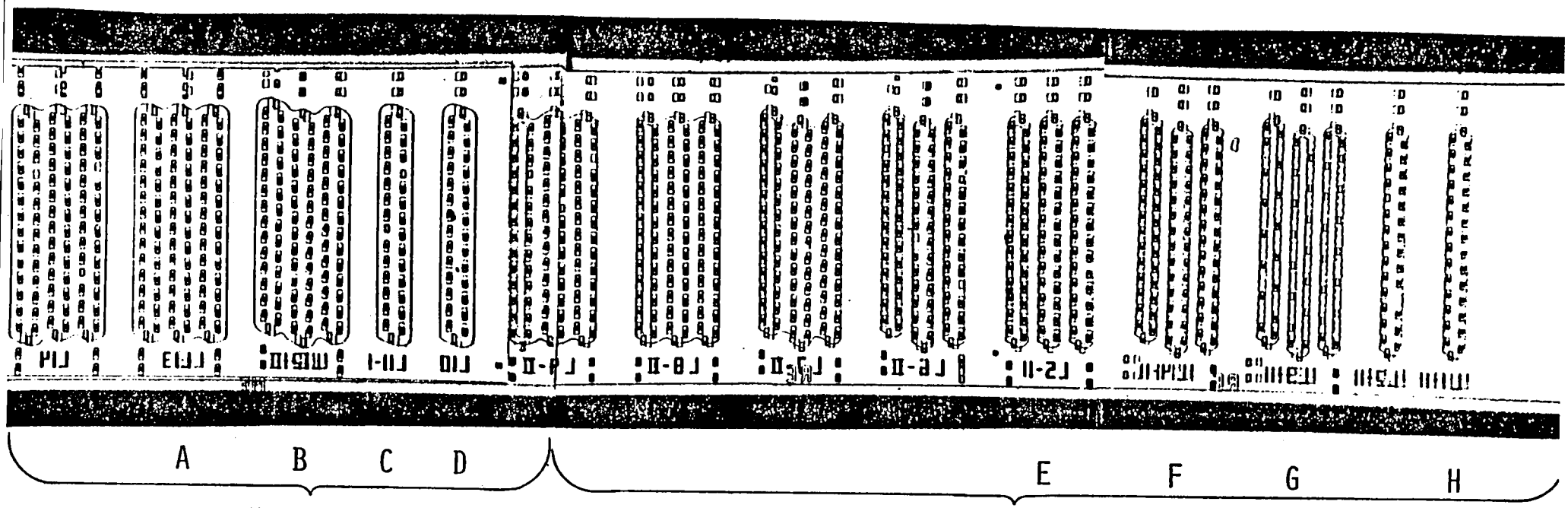
### 3.5.1 Chip II Description:

Chip II is designed to provide further understanding of mesa and recess barriers, in particular with groups of loops compared to the single loops of chip I. Chip II also explores the behavior of self-structured bubble columns slipping past each other as needed for the storage area in a major/minor loop device structure. Finally, chip II tests the defect tolerance aspect of the self-structured approach by having deliberate defects in the propagation lithography.

Chip II was designed with the following features as shown in Figure 3.5.1:

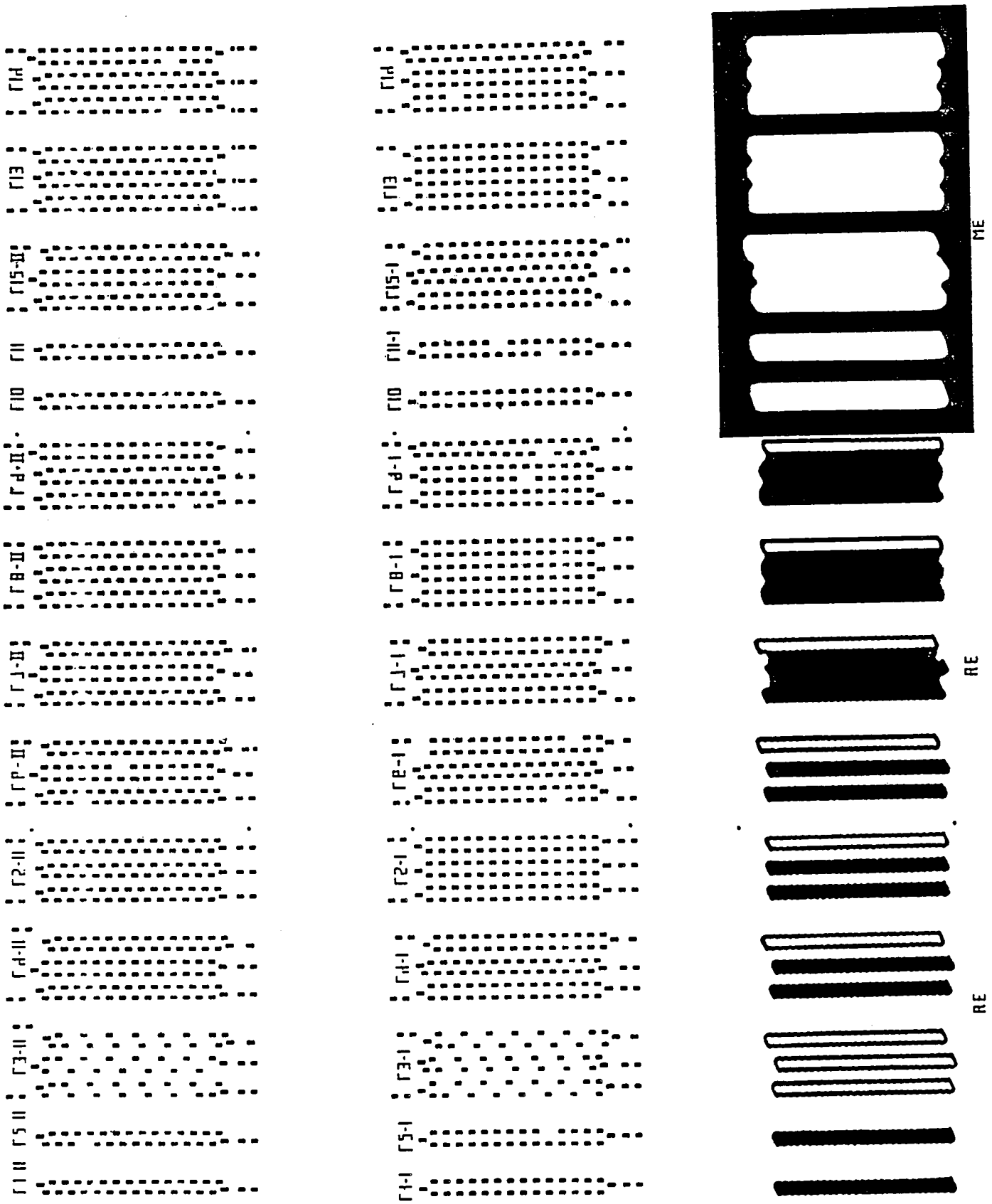
- single propagation loops
- single propagation loops with aperture defects
- triple propagation loops, co-rotating
- triple propagation loops, counter-rotating
- triple propagation loops with aperture defects
- triple propagation loops with 50% aperture defects
- mesa and recess barriers

Figure 3.5.2 shows the individual conductor patterns and barrier milling artwork. Figure 3.5.3 shows details for 1/3 of the chip. The single loops are essentially duplicates of chip I loops for reference as control loops. The single loops and triple loops with aperture defects have single propagation apertures missing in both conductor layers. These are to test the ability of the self-structuring to maintain loop operation despite imperfect fabrication. Counter-rotating and co-rotating loops result in different column slipping environments. In the co-rotating loops, each bubble column has its surrounding columns moving in the opposite direction. This operating mode is the best from an I/O track and gating point of view but puts the bubbles in a structure with the least 'lattice' type support. The counter-rotating loops result in a storage area made up of hexagonal packed, two column wide lattices of bubbles moving together. This gives better lattice support but is less desirable from the I/O track and gating points of view. This is because the ends of the storage loops don't line up when positioned for proper hexagonal positioning of the bubbles. The triple propagation loop group with 50% defects is included as a means, depending on point of view, of testing defect tolerant operation at an extreme level of defects or testing whether operation would work well with propagation elements only at every other storage cell.



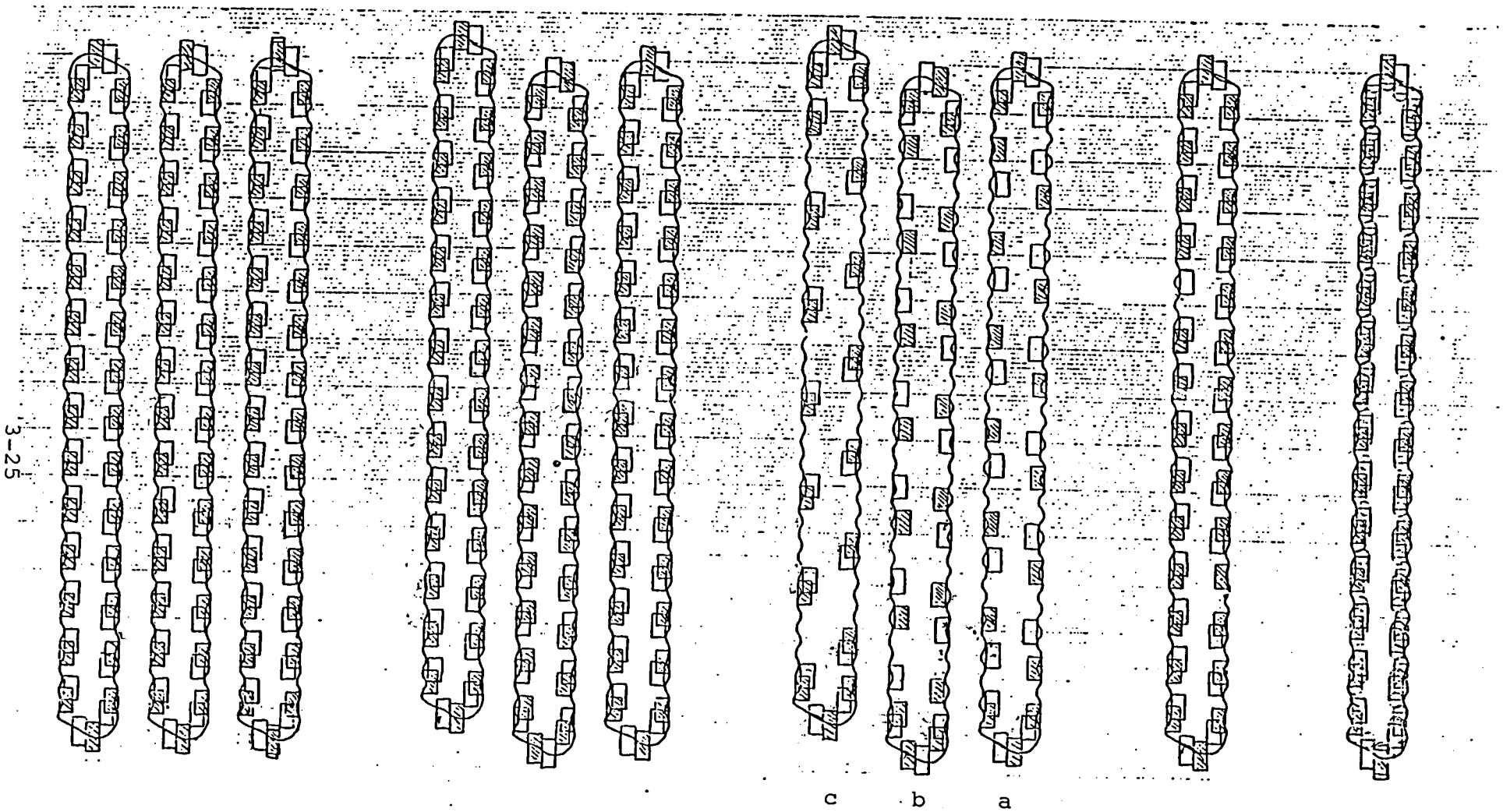

A - COUNTER-ROTATING GROUP OF THREE LOOPS WITHIN A SINGLE BARRIER
B - CO-ROTATING GROUP OF THREE LOOPS WITHIN A SINGLE BARRIER
C - SINGLE LOOP WITH INTENTIONAL MISSING APERTURES
D - MESA BARRIER CONTROL LOOP
E - COUNTER-ROTATING GROUP OF THREE LOOPS WITH SEPARATE BARRIERS
F - CO-ROTATING GROUP OF THREE LOOPS
G - LOOPS WITH 50% INTENTIONAL DEFECTS
H - RECESSED BARRIER CONTROL LOOP

FIGURE 3.5.1 COPY OF COMPOSITE PHOTOGRAPH OF CHIP 2 WITH REPRESENTATIVE FEATURES LABELED.




Barrier and propagation layer artwork for Chip II. Dark areas are where garnet is milled for barriers or aluminum is milled for apertures.

Figure 3.5.2




1/3 of Chip II showing details of recess barriers and propagation conductors. In particular, the two versions of 50% defects is shown. Loops a & b functioned better than c.

Figure 3.5.3

### 3.5.2 Chip II Fabrication:

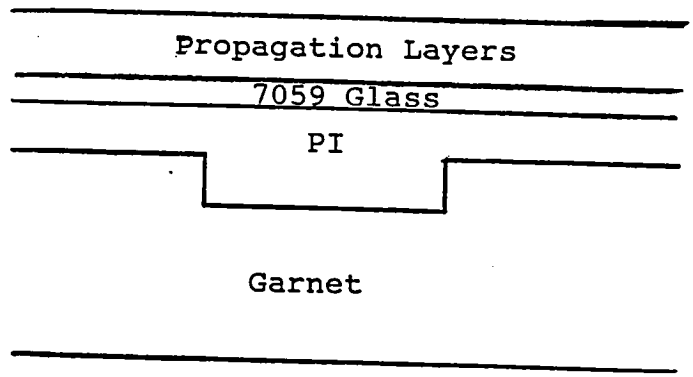
In the chip II's fabricated, apertures are generally 6μm by 12μm, and the bubble diameter is in the 5μm to 6μm range. The propagation conductors were made from either evaporated Al, or Al-4% Cu, or sputtered Al.

Chip II samples were fabricated in three different structures with regard to barrier step shape and spacer dielectric material. Figure 3.5.4 illustrates the approaches. The key concern is to obtain a sufficient discontinuity in the garnet thickness to provide a good barrier and yet obtain continuous propagation conductors across the barriers. The three structures fabricated are: abrupt barrier steps with a polyimide glass planarizing spacer covering (3.5.4a), abrupt barrier steps with glass spacer covering (3.5.4b), and profiled barrier steps with glass covering (3.5.4c). Details on the 'a' and 'c' structures are presented in Appendix A.

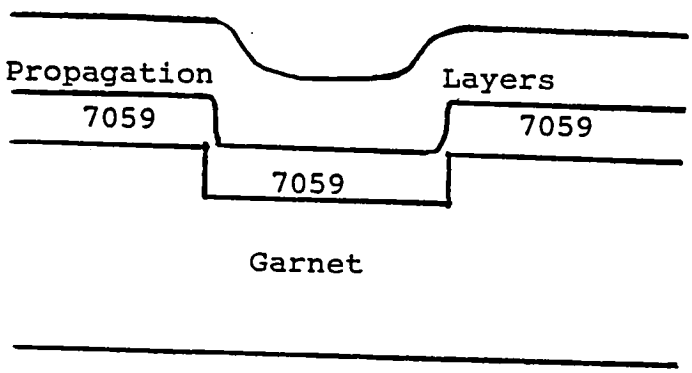
The simplist structure to fabricate with consistent results is the abrupt garnet step with a glass spacer (3.5.4b). Unfortunately, this structure functions poorly from the discontinuities in the propagation conductors when crossing the barrier steps. Changing from evaporated Al conductors to sputtered Al with better step coverage capability didn't cure this problem. Besides making propagation in the storage area operate poorly, this structure gives the illusion that the barrier also works very poorly. The reason is shown in Figure 3.5.5.

Because of the discontinuities or at least reduced thickness of the propagation conductors over the barrier, the propagation current tends to flow around the loop areas as shown in 'A'. One effect of this difference in current flow is to create unequal magnetic potential energy wells from the apertures on the inside versus the outside of the barrier. This results in bubble propagation which removes bubbles from the propagation loop as shown in "B". The outside pole #3 is sufficiently stronger then the inside pole #3 to overcome its separation disadvantage and attract bubbles across the barrier. A second effect of the distorted current flow is to increase the current density near the edges of the conductor. This is due first, directly to the distorted density, and secondly, because the average current density must be increased to get adequate current density in the deprived areas inside the barriers. The overall result is to increase the conductor edge effects which cause bubbles to strip out and propagate poorly. These edge effects are particularly disruptive on chip II because propagation loops cover a relatively large percentage of the conductor width to enable better study of slipping columns of bubbles when propagating.

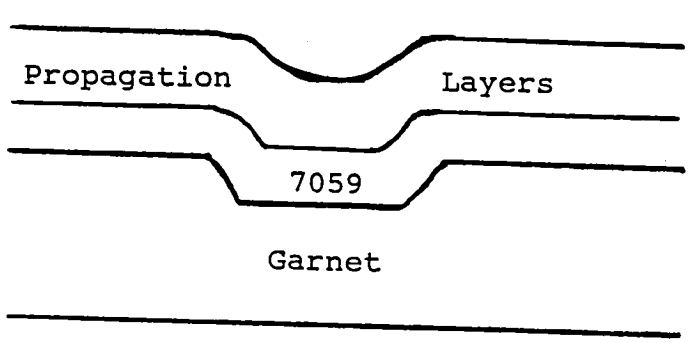
a) Abrupt barrier step with PI/7059 spacer




b) Abrupt barrier setp with 7059 glass spacer

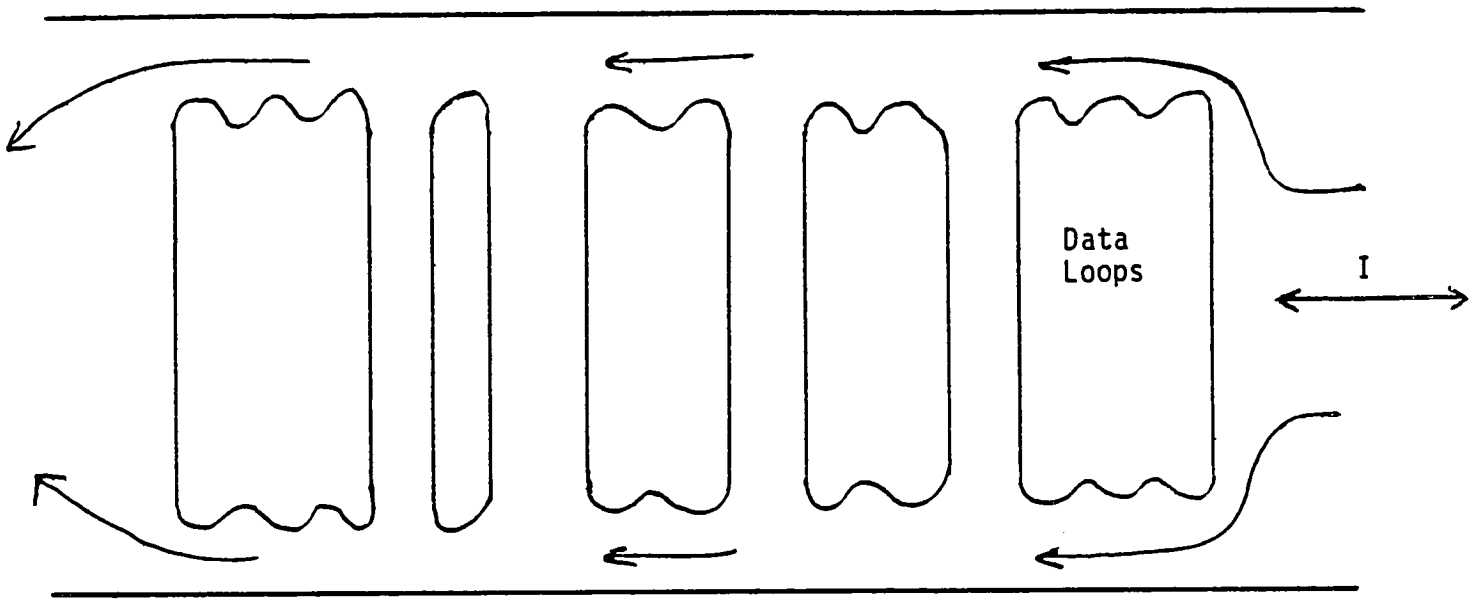



c) Profiled barrier step with 7059 glass spacer

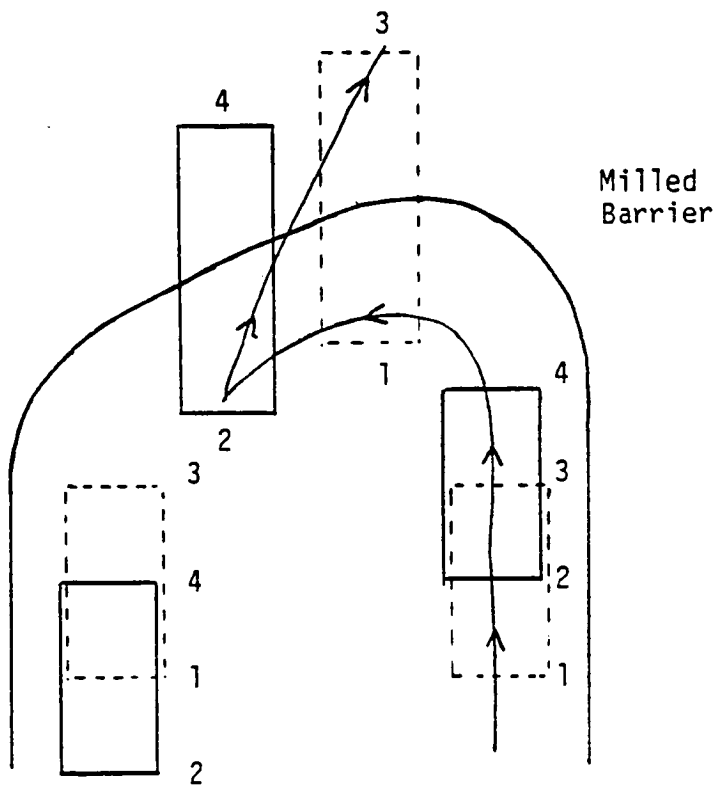



Garnet barrier/spacer layer structures used in Chip II to test barrier and propagation performance.

Figure 3.5.4




A - Current flow diversion around barrier enclosed data loops.




B - Removal of a bubble from the data loop due to unequal pole strengths inside and outside the barrier.

Figure 3.5.5

As a result of the poor conductor behavior, no generally useful results were obtained using the 3.5.4b structure.

The 3.5.4c structure with profiled barrier steps gave occasionally good results for barrier steps of less than ~0.4 micron. The greatest difficulty with this structure is the poor repeatability in profile shape and the difficulty in making timely, accurate measurements of the shape. SEM photographs and Dektak II profilometer measurements were used to monitor the results as discussed in Appendix A. At barrier heights greater than ~0.4 microns, the garnet step became more like the abrupt 3.5.4b structure and its problems. Samples with this structure were not used extensively for propagation and barrier testing.

The 3.5.4a structure with polyimide glass covering abrupt barrier steps resulted in the best samples. This general approach was the first taken early in the contract when polyimide alone was used as the spacer layer in initial Chip I fabrication. Problems with blistering, peeling and wire bonding from polyimide outgassing resulted in the 3.5.4b and then 3.5.4c approaches being used first on chip II. During that time, improved polyimide materials were developed by vendors such as Hitachi with which we fabricated the successful 3.5.4a structure.

The polyimide glass spacer worked well as a base for subsequent fabrication. Bubbling and peeling were not problems and neither was wire bonding to the conductors deposited on this base.

As a side note, the use of this planarizing spacer is not planned for future device fabrication when mil spec temperature ranges will be a concern. At that point, ion implantation to provide barriers by damaging rather than removing appropriate volumes of garnet will be used to provide barriers and a planar surface.

### 3.5.3 Chip II Testing:

The various arrangements of loops and barrier in chip II all showed relatively equivalent performance. Both recess and mesa barriers were effective at keeping bubbles contained in their loops or groups of loops. Additionally, for those groups of loops with a single common barrier, both co-rotating and counter-rotating movement of bubbles (one loop relative to the next) showed good stability of column motion. This stable motion (no jumping between loops) was even maintained at positions where deliberate defects in the propagation structure could have upset the movement. Figures 3.5.6 and 3.5.7 show propagation margins for the mesa and recess loops. Overlapping and non-overlapping pulses refers to whether the propagation pulses were overlapping temporally by 33% or were separated with no overlap.

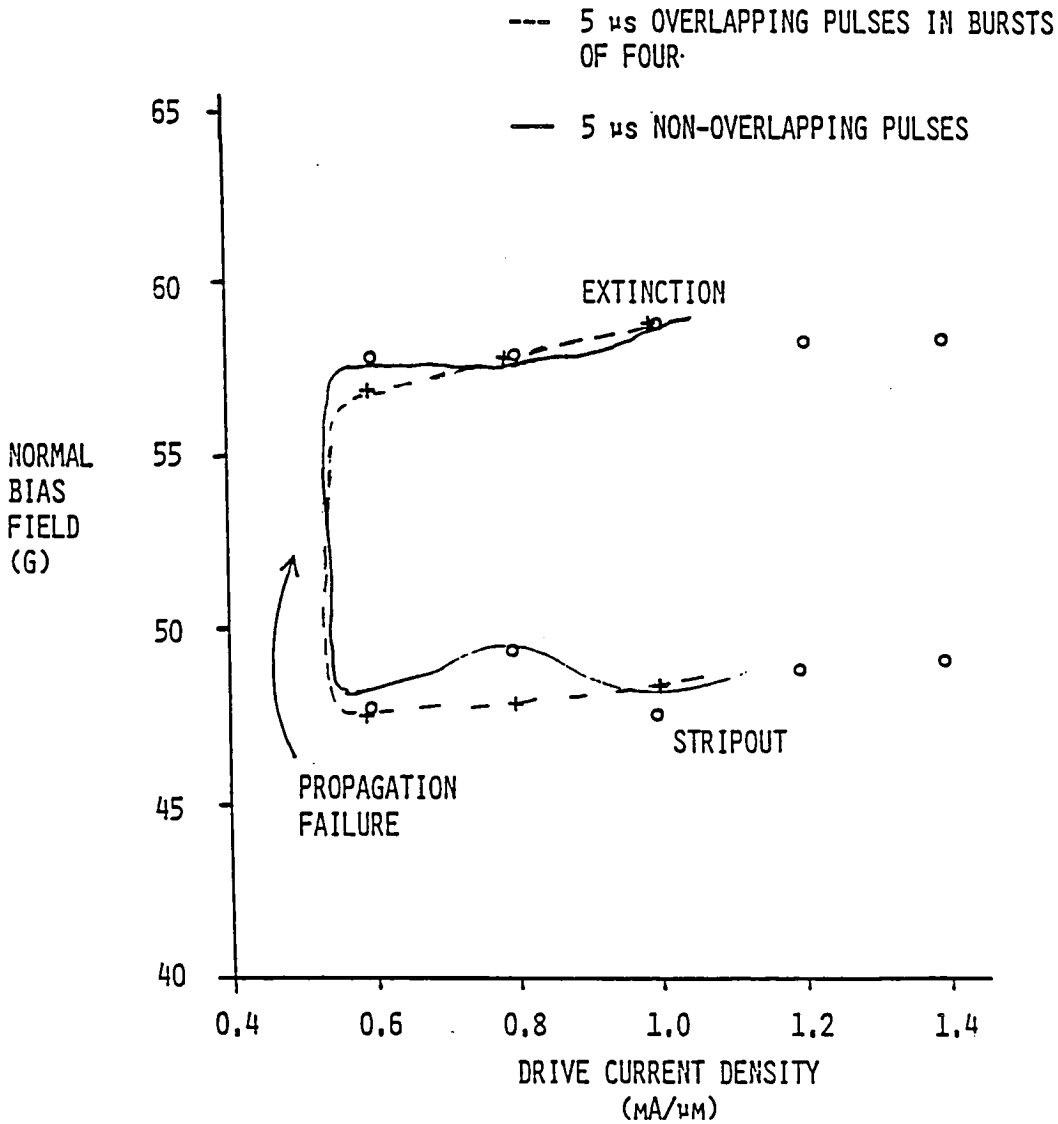



FIGURE 3.5.6 PROPAGATION MARGINS FOR MESA BARRIER CONTROL LOOP IN CHIP 2 (SAMPLE 2061) FOR OVERLAPPING AND NON-OVERLAPPING DRIVE PULSES.

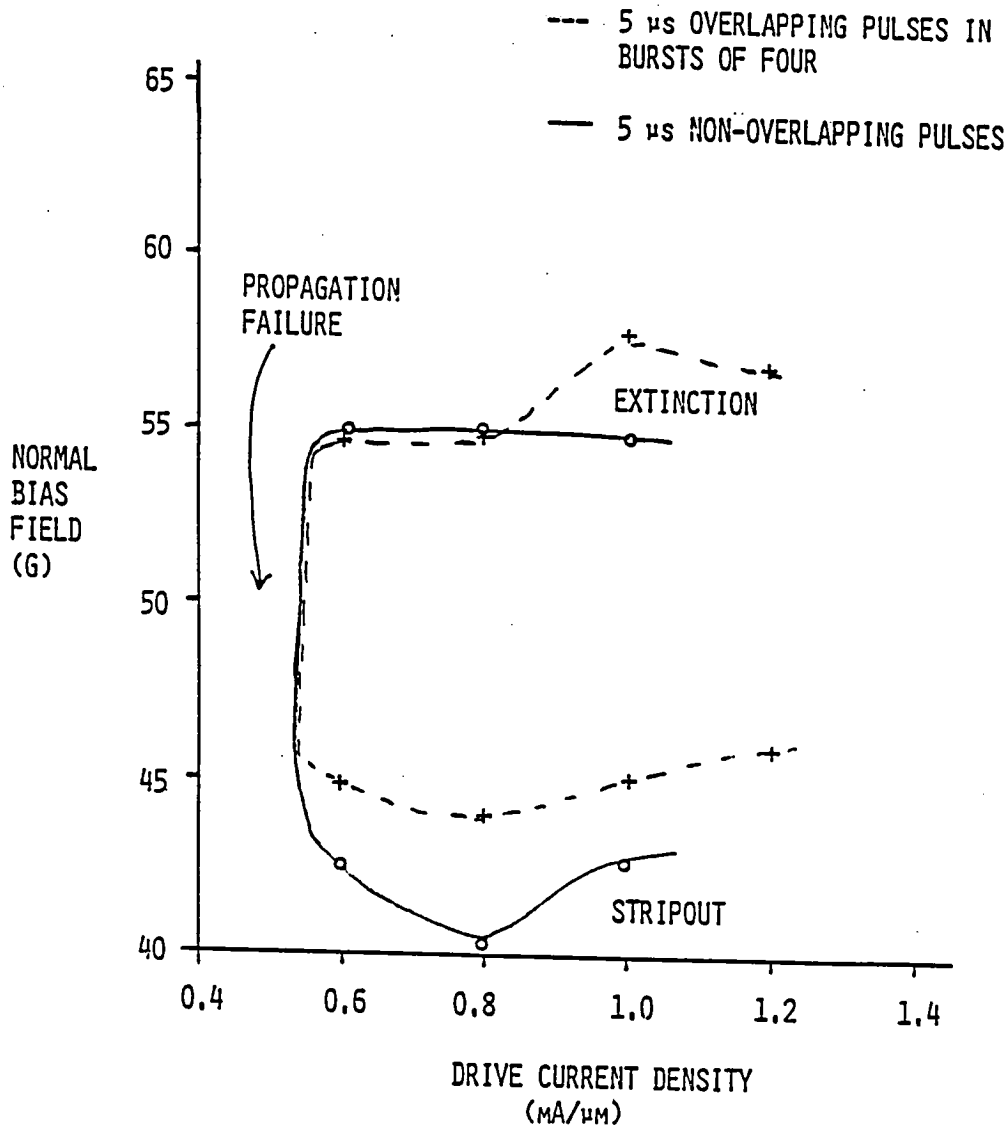



FIGURE 3.5.7 PROPAGATION MARGINS FOR RECESSED CONTROL LOOP IN CHIP 2 (SAMPLE 2061) FOR OVERLAPPING AND NON-OVERLAPPING PULSES.

The primary loss of bubbles from the loops occurred at the ends where fields from the edge of the propagation conductors would strip or collapse bubbles depending on drive current levels and bias field magnitude. The loss rate from these effects was low enough that good observations of fully populated loops could be made. In a memory device, these edge effects would not be present due to cancellation by return conductors and will not be a problem.

The operation margins shown in 3.5.6 and 3.5.7 for triple loops is essentially identical to the margins for single loops and in both cases were unaffected by the deliberate propagation defects. The significance of this result is that it demonstrates that neighboring columns of bubbles can be propagated at a self-structured density in a lattice slipping mode. This combined with the good performance of the co-rotating loops indicates major/minor loop architectures similar to conventional chips are possible while obtaining the densities and defect tolerance benefits of the self-structured approach.

Good results were also obtained for the group of loops with 50% intentional propagation defects. This was included to test, depending on perspective, an extreme level of fabrication defects in a device which nominally would have propagation structure at all bubble positions or a propagation design with structure at only half the bubble positions. In either case, the loop propagated bubbles successfully although with smaller margins then fully structured loops and with much greater dependence on having bubbles at every position. This successful propagation confirms that the self-structured approach does provide good defect tolerance in storage areas. This could allow memory devices which have good production yields without the need for redundant loops with their corresponding added control overhead and loss of effective device area. If a reduction in the number propagation features is desired instead, these results indicate that good possibilities exist for this approach despite there being no stripe domains and having bubbles slipping past one another as in a fairly conventional architecture.

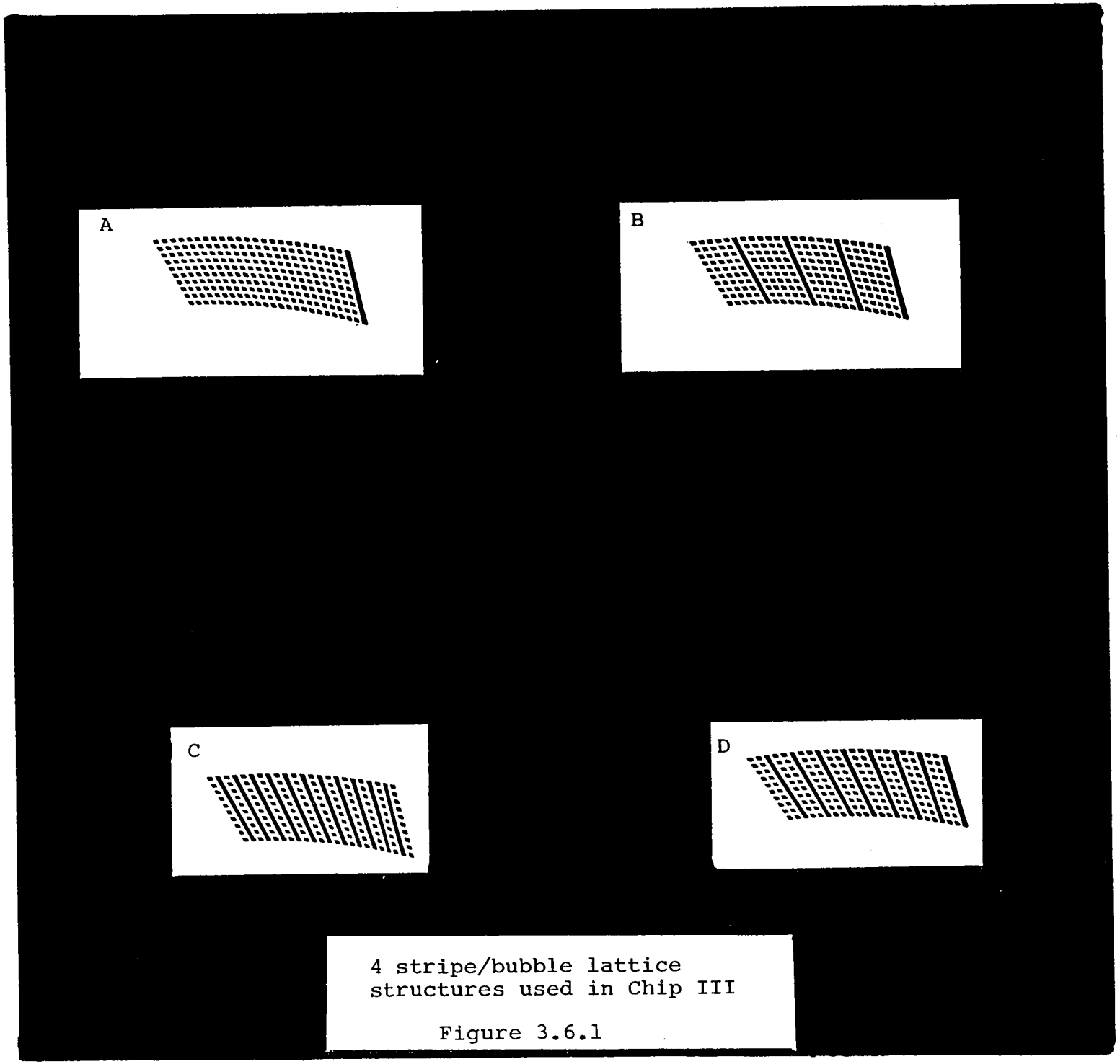
## 3.6 Chip III - Circular Storage Area, Strip-Bubble Non-slipping Lattice

### 3.6.1 Chip III Description:

The basic concept of this chip is to propagate stripe and bubble domains in a circular circuit with multiple apertured conductors. This results in storage areas in which no slipping motion of bubble columns is used and which have varying densities (from 0 to 50%) of stripe domains to maintain order of the lattice.

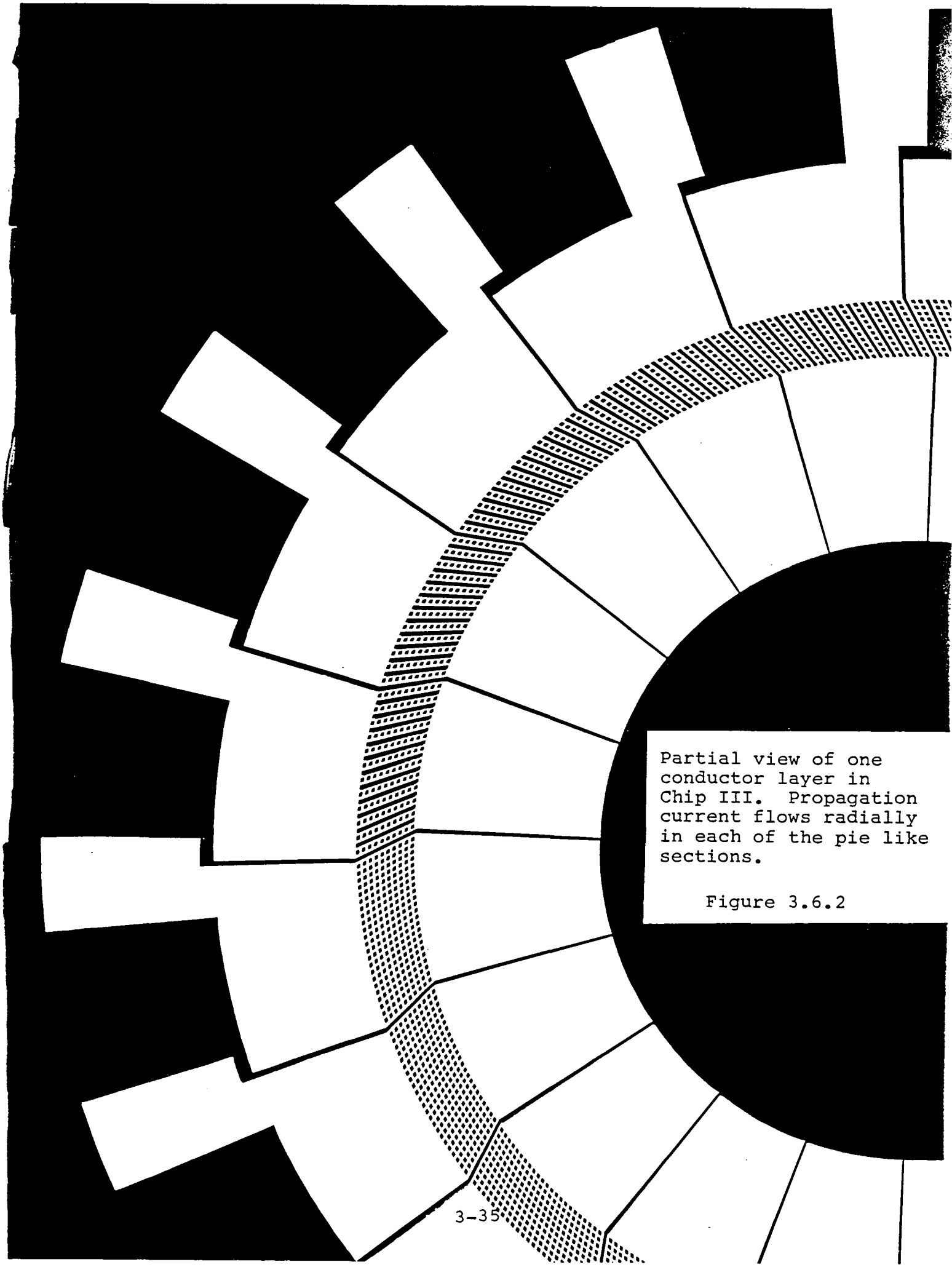
Figure 3.6.1 shows the lattice domain patterns used in the chip. Pattern 'A' would have nearly 100% bubbles with a stripe present only once per pie shape propagation section (Figure 3.6.2). Pattern 'B' has five columns of bubbles for every stripe domain, pattern 'D' has two columns of bubbles for every stripe domain, and pattern 'C' has only one column between stripes. These patterns determine what domain pattern is generated when a current pulse is used to generate stripes and bubbles. One of the central questions for this chip was to see whether stripes were needed, and if so to what extent, to maintain stability in the bubble positions. All of the 3.6.1 patterns used in chip III position bubbles in hexagonal lattice positions and maintain that pattern during propagation.

These lattice patterns were placed end to end to from a complete circular path of which Figure 3.6.2 shows nearly one half for one of the conductor layers. As shown, the individual conductor layer is made up of roughly pie shape sections and the propagation current flows radially in these sections. The entire chip is made up of four conductor layers which include return planes and via interconnects to form a complete electrical circuit. One propagation layer (two conductor layers) is shown in Figure 3.6.3. The current flow can be followed by starting at the via at position 'a'. Here the current enters the propagation section centered in the figure by flowing away from the via at 'a' towards the via at 'b'. Along the path it crosses the propagation structure. The patterning looks unusual in this figure because the return conductor also is patterned to match the incoming conductor but with an aperture width circumferential shift to accommodate the opposite current flow directions in the two layers. At via 'b' the current flows from the incoming conductor to the return conductor and then towards via 'c' which is equivalent to via 'a' by symmetry for the next propagation section. Continuing in this way, the current flows around the entire circle made up of twenty propagation sections. The second propagation layer (3rd and 4th conductor layers) is the




4 stripe/bubble lattice structures used in Chip III

Figure 3.6.1



Partial view of one conductor layer in Chip III. Propagation current flows radially in each of the pie like sections.

Figure 3.6.2

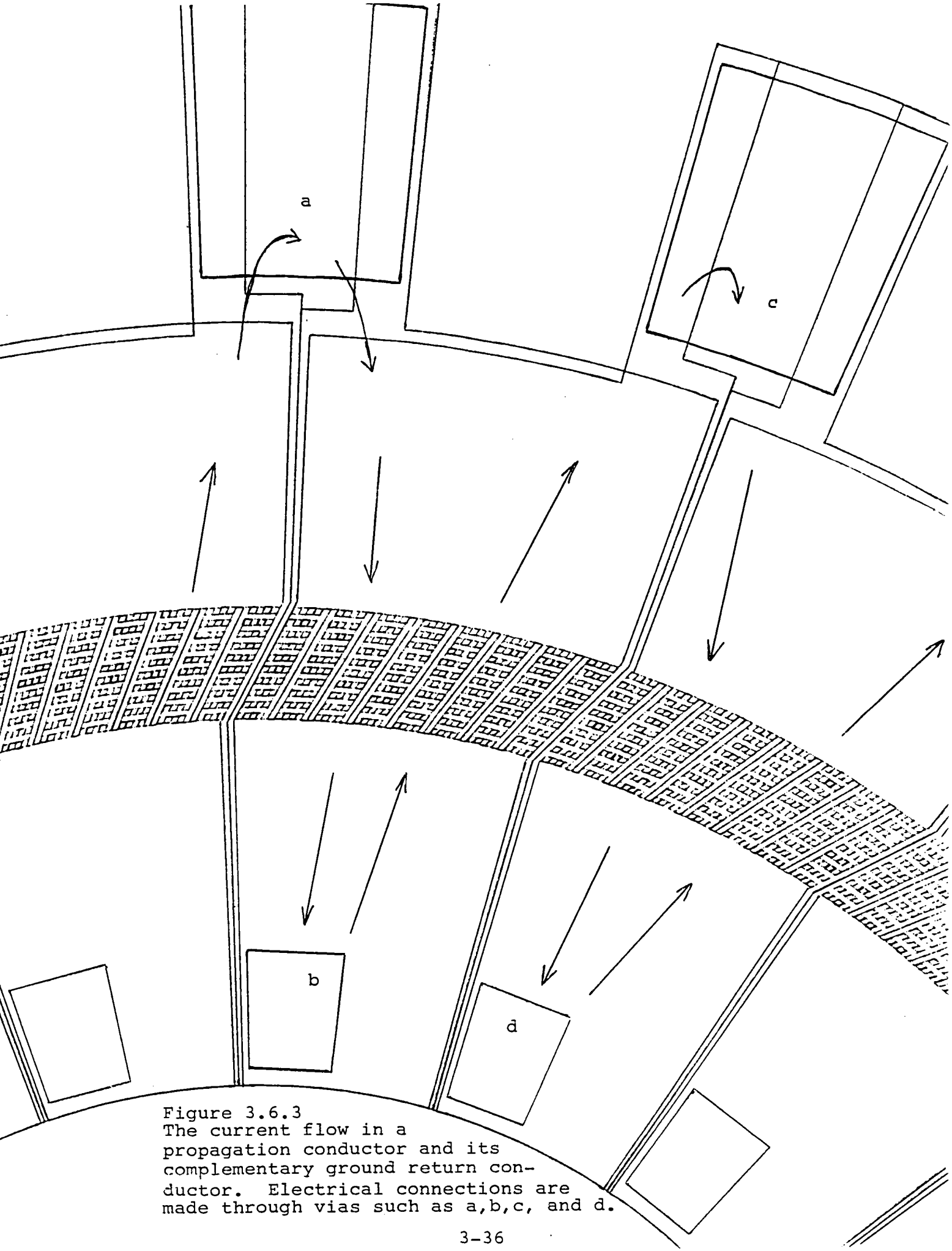



Figure 3.6.3
The current flow in a propagation conductor and its complementary ground return conductor. Electrical connections are made through vias such as a,b,c, and d.

same except for being rotated nine degrees circumferentially. This results in an interleaving of the vias and connection pads for the two propagation layers. A pair of larger 'feet' were provided for each propagation layer to make external electrical connections and to break the circle electrically. Note in both propagation layers, the edges of the individual pie shape sections are positioned to be equivalent to a stripe via.

### 3.6.2 Chip III Fabrication:

This chip presented fabrication difficulties different from chips I and II. In particular, the dependence on a fairly large number of vias through which good electrical connections are required between conductor depositions made obtaining a fully workable chip difficult. While the fabrication processes were being improved to successfully build a complete chip III but before one was, successful results from chips I and II resulted in this approach being put on hold in favor of investigation of chip I and II approaches.

### 3.6.3 Chip III Testing:

As a result of this approach being put on hold no testing results were obtained for chip III.

## 3.7 Chip IV - Circular Storage With An I/O Track

Chip IV design was not built or tested since the chip III effort was abandoned.

## 3.8 Chip V - I/O Tracks, Gates and Generators

### 3.8.1 Chip V Description:

Chip V was the first test chip design to use the major loop (I/O track) - minor loop (storage loop) concept for self-structured bubble storage and control. The geometry of each of the three conductor layers is shown in Figures 3.8.1a (first propagation layer), 3.8.1b (second propagation layer) and 3.8.2 (control conductor layer). Figure 3.8.3 shows the two propagation layers together. The superposition of both propagation layers and the control conductor layer is shown in Figure 3.8.4. A schematic layout of chip V is given in Figure 3.8.5.

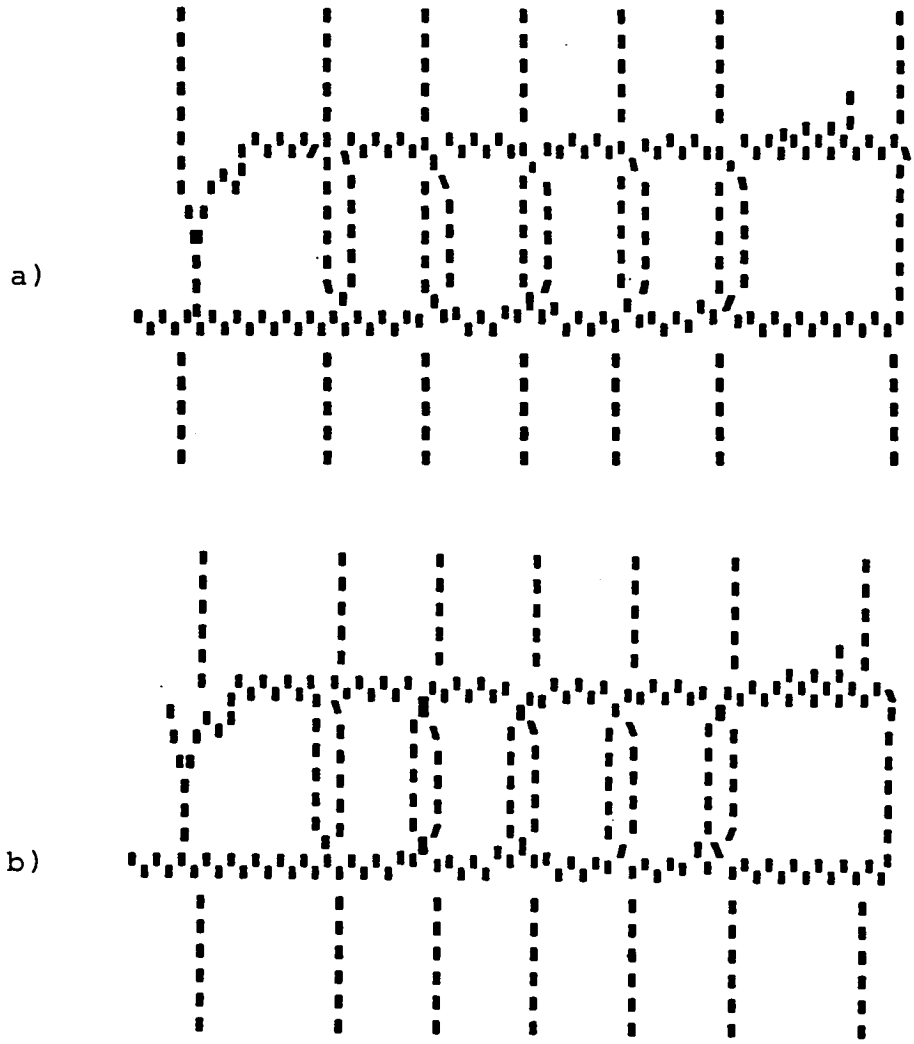
The overall purpose of the chip was to test initial designs of the I/O track, generators and a variety of gates. The gates include transfer, swap and replicate functions for storage loop-I/O track connection, I/O track to I/O track transfer and swap, and I/O track merging.

As with all circuits in this study, bubble propagation was accomplished with apertured dual conductors. The gates were designed to use the two drive conductors and/or a third conductor for bubble control. The standard apertures in chip V were 6 microns by 12 microns for use with 5 to 6 micron diameter bubbles.

General descriptions of the component set (gates, detectors, generators, etc.) included in the chip V design are given in Section 2.3 of this report.

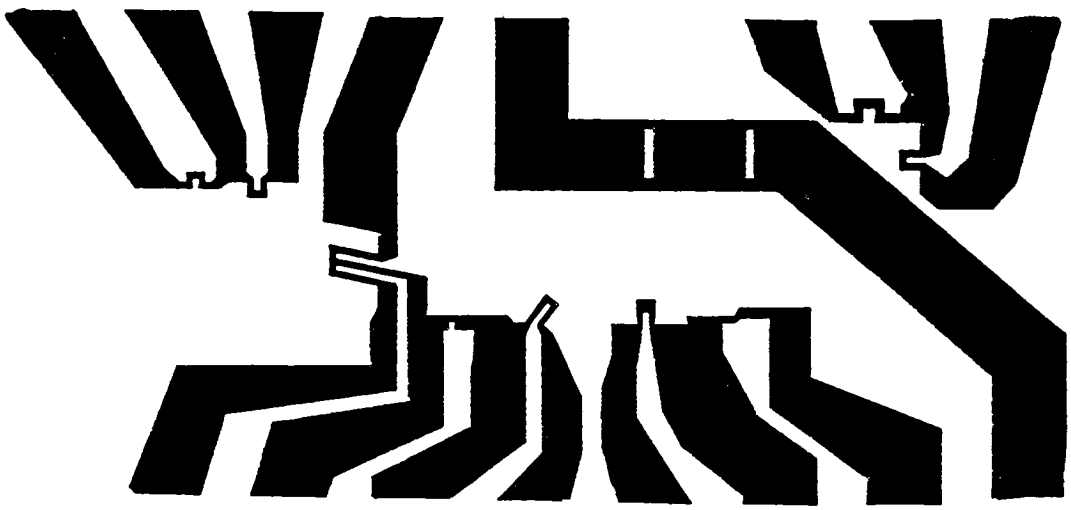
There were four hairpin generators in chip V (see Figures 3.8.2 and 3.8.5). Six micron wide conductors and a six micron wide gap were used for three of them. The fourth generator had ten micron dimensions (generator 3 at location 9 in Figure 3.8.5).

Two replicate gates were designed for chip V. Replicate gate 14 (Figure 3.8.5) was designed to use a small ion implanted area as discussed in Section 2.3.6. Ion implantation was not available at processing time and therefore was not included in the fabrication process. Replicate gate 15 used a set of nested drive apertures. It was noted after the chip V masks were made that this gate would not replicate bubbles. Hence this gate was only studied as a set of short nested drive sequence control gates (similar to gate 5).



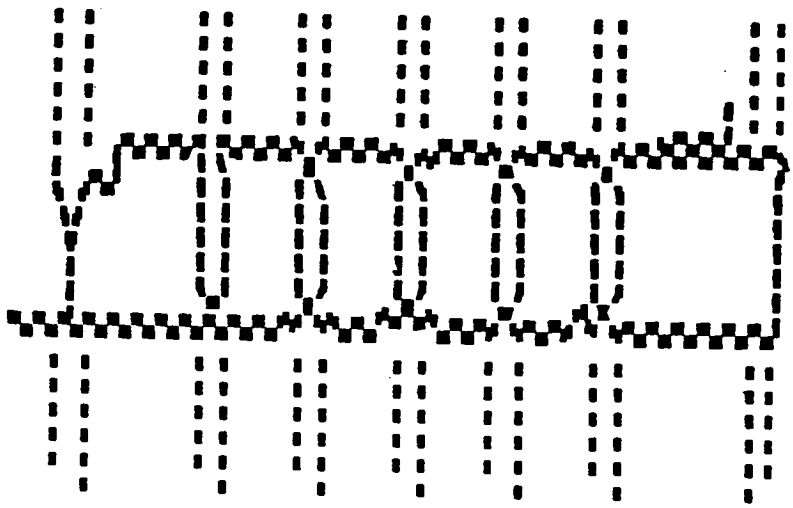

Aperture layout for Chip V propagation conductors.

Figure 3.8.1



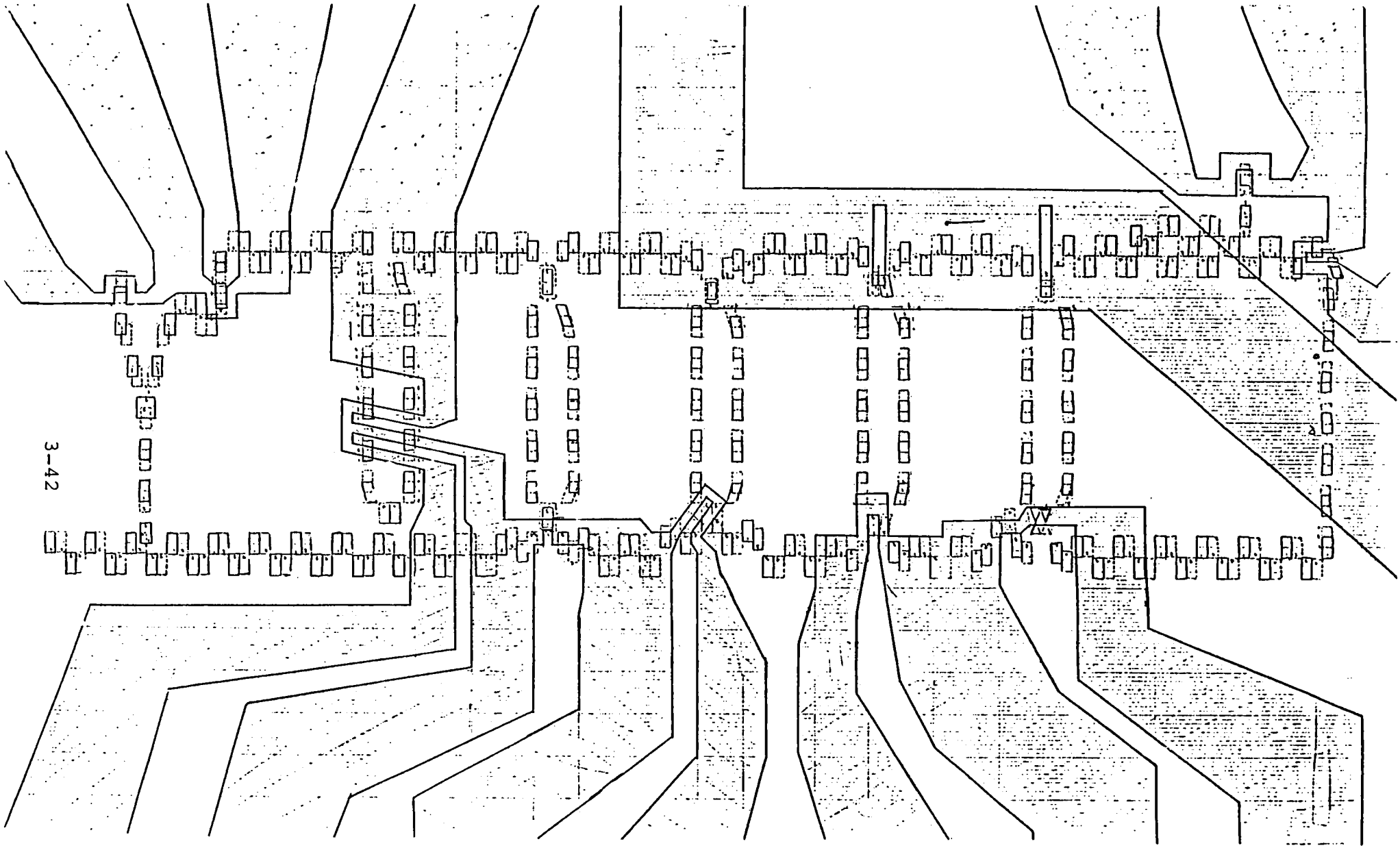
Chip V control conductors.

Figure 3.8.2



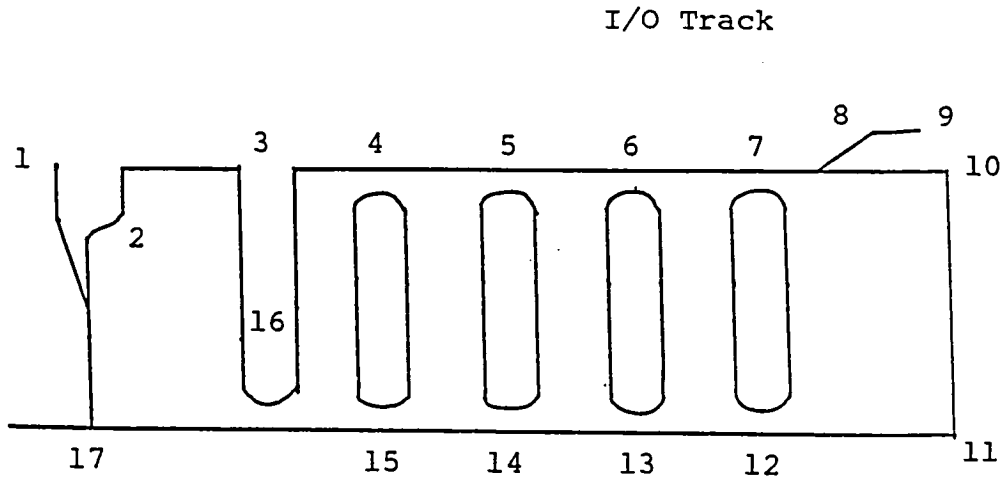
Chip V propagation conductor layers superimposed.

Figure 3.8.3



Superposition of both aperture drive layers and the control conductors for Chip V.

Figure 3.8.4




1 - generator 1
2 - generator 2
3 - I/O track square corners
4 - sequence controlled transfer gate 1 (with long apertures)
5 - sequence controlled transfer gate 2 (with short apertures)
6 - aperture control conductor transfer gate 1
7 - aperture control conductor transfer gate 2 (with nested drive apertures)
8 - merge gate 1
9 - generator 3 (larger hairpin)
10 - generator 4
11 - square corner
12 - control conductor swap gate
13 - hairpin transfer gate
14 - hairpin replicate gate (for use with ion implant area)
15 - replicate with nested drive apertures (non-functional as replicate)
16 - control conductor swap gate
17 - merge gate 2
18 - merge gate 3

Chip V Schematic Layout and Feature Identification

Figure 3.8.5

It should be noted here that while gate 12 (Figure 3.8.5) was designed as a control conductor swap gate, it also demonstrates a phase matching corner. In this mode, there is no current applied to the control conductor and there is no transfer of bubbles across the gate. This is shown in Figure 3.8.6. The use of this phase matching corner allows the use of oppositely rotating storage loops as compared with the normal storage loop. This is again used effectively in chips VI and VII of this study.

### 3.8.2 Chip V Fabrication:

All of the chip V testing was done on samples using the following fabrication layers:

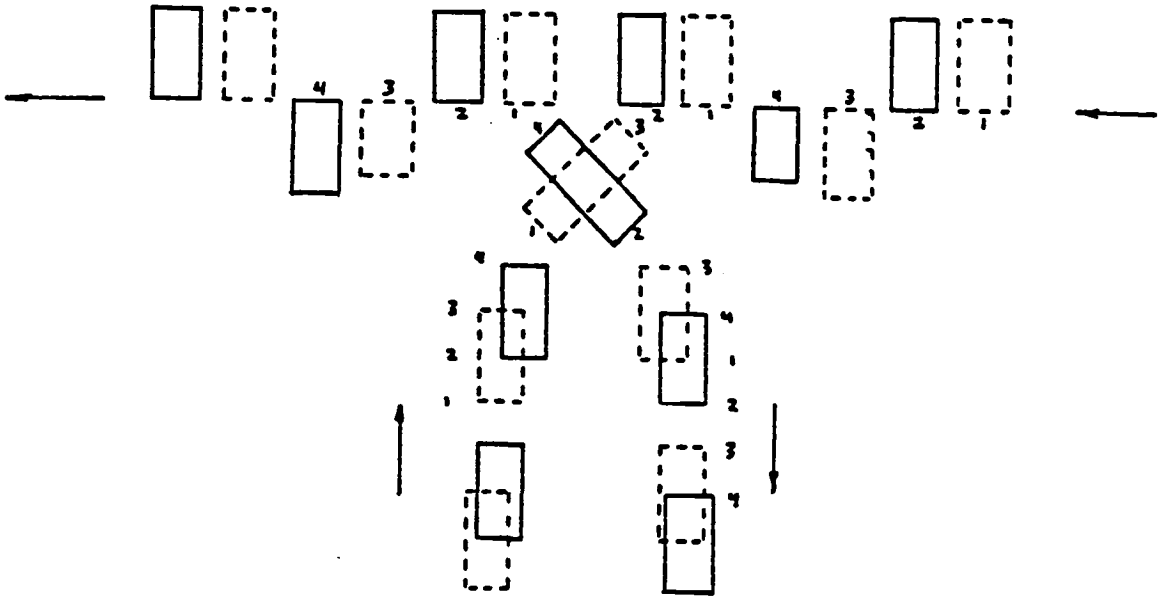
1. SiO spacer layer
2. 1st. drive layer - Al/4%Cu
3. Chrome etch stop
4. Glass [14]
5. 2nd. drive layer - Al/4%Cu
6. Chrome etch stop
7. Glass
8. Control conductors - Al/4%Cu

### 3.8.3 Chip V Testing:

Storage Loops

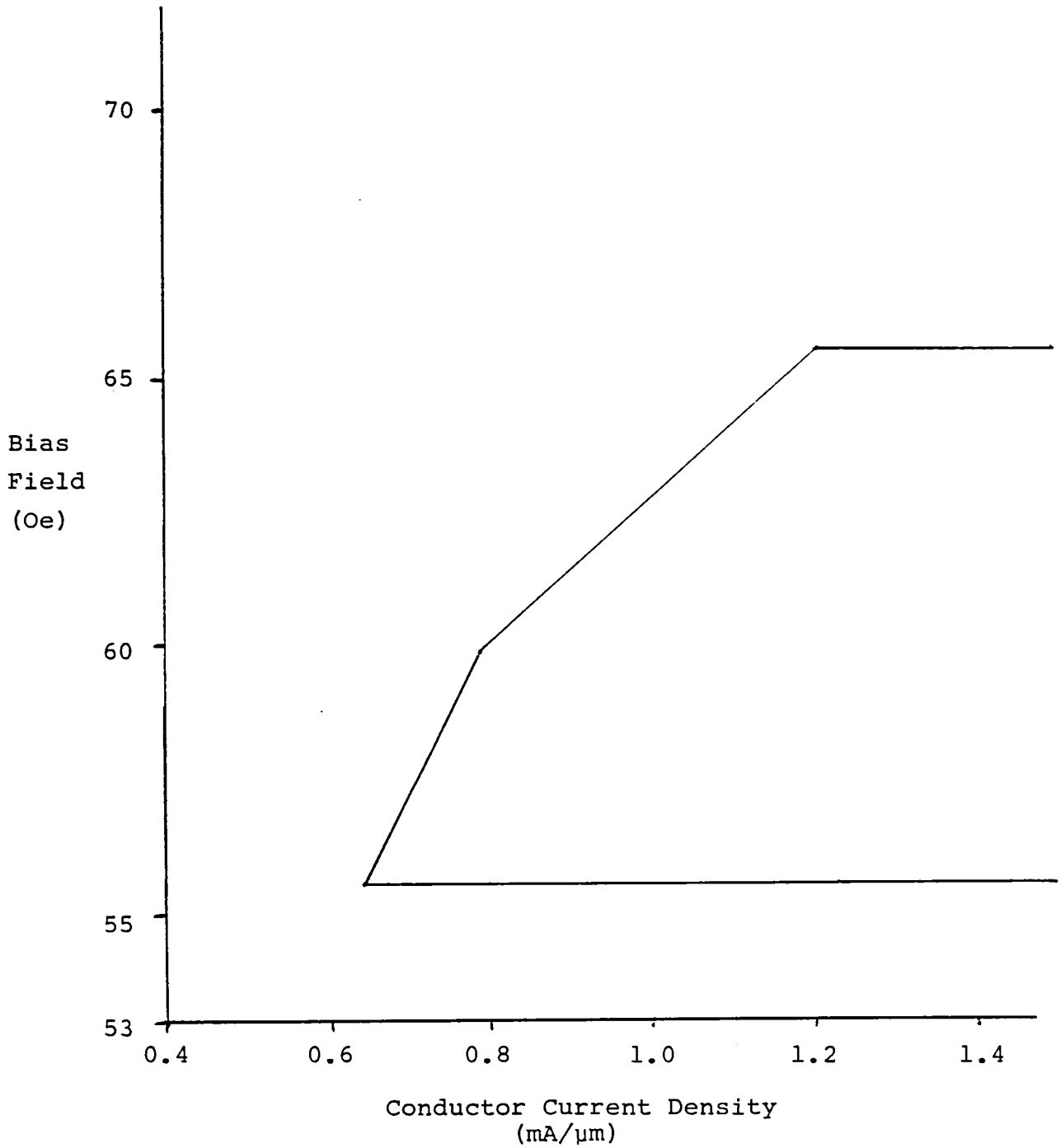
Storage loops of chip V were tested to establish the operating margins of applied bias field vs apertured conductor current. Figure 3.8.7 illustrates the operating margins for a simple propagation loop, where bubble propagation was promoted by non-overlapping 5μsec wide pulses in the two apertured conductors. The lower bias field margin was limited by bubble strip-out, and the upper margin by bubble collapse or ejection from the circuit.

The same propagation loop was evaluated for bubble propagation margins utilizing 6μsec wide pulses with a 33% overlap (Figure 3.8.8). Bursts of four overlapping pulses were applied to the circuit at a low repetition rate. Figure 3.8.9 illustrates the operating margins. The lower bias field margin at low conductor currents ('A') was limited by bubble strip-out, and at high conductor currents ('B') by ejection from the circuit at the corners. The



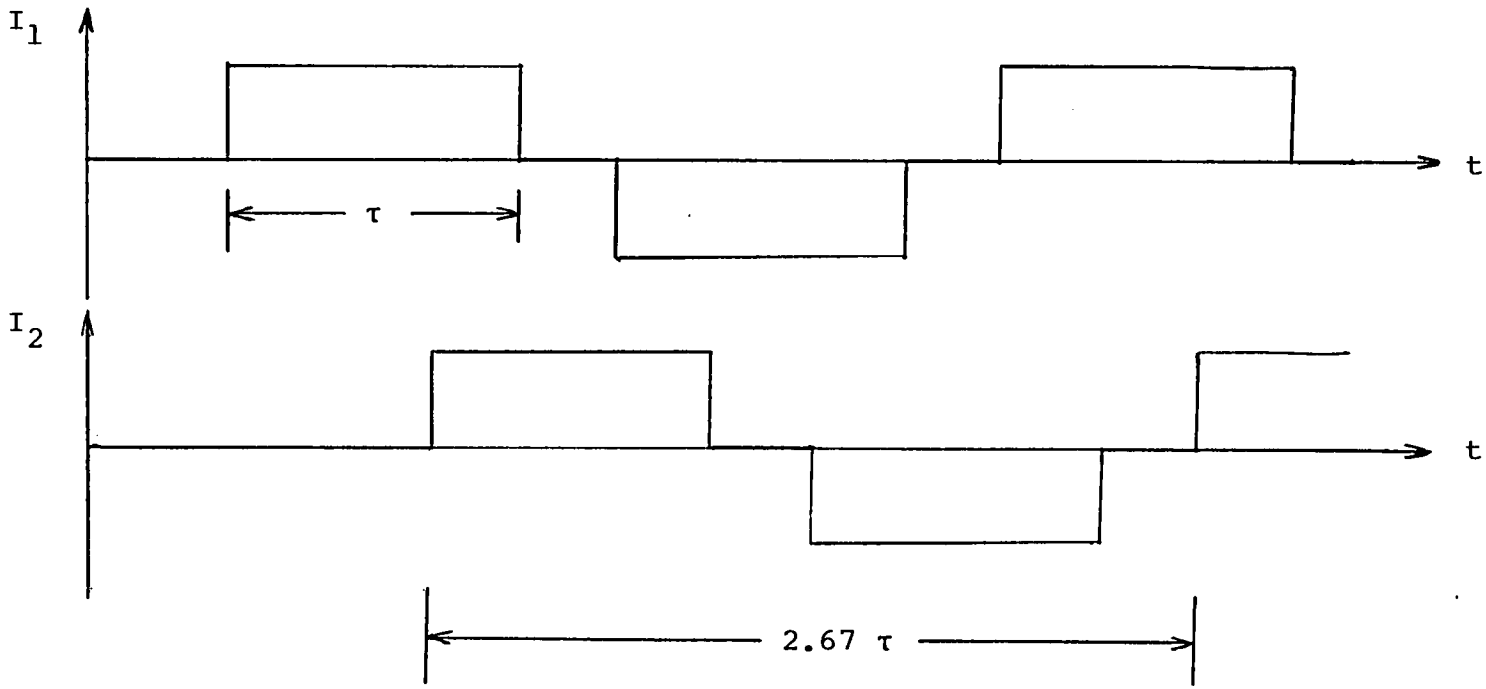
Phase matching corner.

Figure 3.8.6



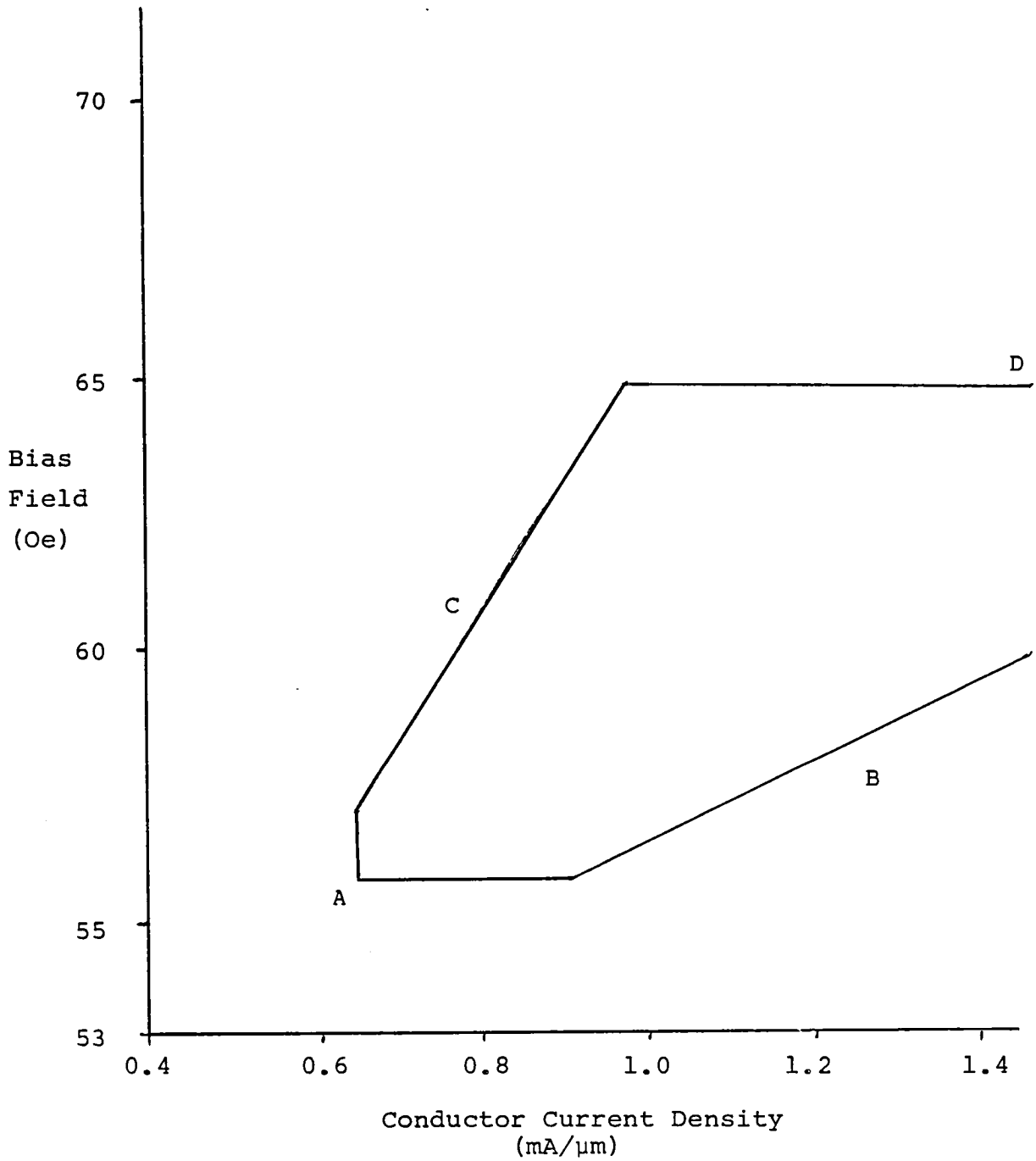

Chip V bubble propagation margins with 5μs non-overlapping pulses.

Figure 3.8.7




Pulse pattern for dual conductor propagation with overlapping pulses.

Figure 3.8.8




Chip V bubble propagation margins with 6μs overlapping pulses.

Figure 3.8.9

upper margin was limited by ejection at low conductor currents ('C'), and by bubble collapse at high conductor currents ('D'). A majority of the failures occurred at the corners of the loop. This indicated that the behavior of the ends of the loops could be improved with further optimization of the design.

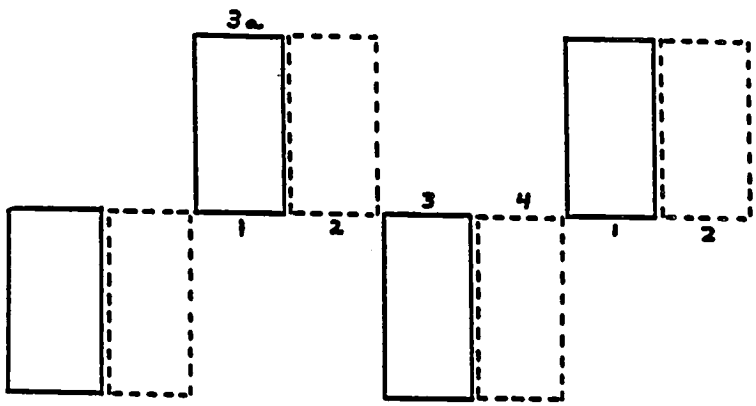
Propagation of bubbles around the minor loops of chip V was also accomplished at higher speed. Again a set of four overlapping pulses was utilized to advance bubble domains one period (wavelength) of the propagation aperture pattern.

Bubble propagation was observed with pulses 0.6μs wide over a current density range from 1.0 to 1.6 ma/μm, and was not observed with 0.5μs pulses. The pulse shape was not ideal, since there was a considerable rise time of 80 to 100 ns. With 33% overlapping pulses, the period for four pulses is 2.67 times the length of one pulse. Therefore, the bubbles were propagating at a 0.62 MHz rate.

The pattern period on the circuit is 25.4μm, and propagating at a 0.62 MHz rate results in an apparent limiting bubble velocity of approximately 16 meters/sec. This is a typical value for the garnet material used for this application. When 2 μm bubble material is employed, rather than the present 5 to 6 μm material, the propagation period will be smaller and, therefore, the propagation rate should increase to 1.5 MHz for the same limiting bubble velocity. Data in the literature [ 2 ] indicates reduced operating margins at 1.43 MHz for an 8 μm period dual conductor circuit, and represents a limiting velocity of approximately 11 meters/sec.

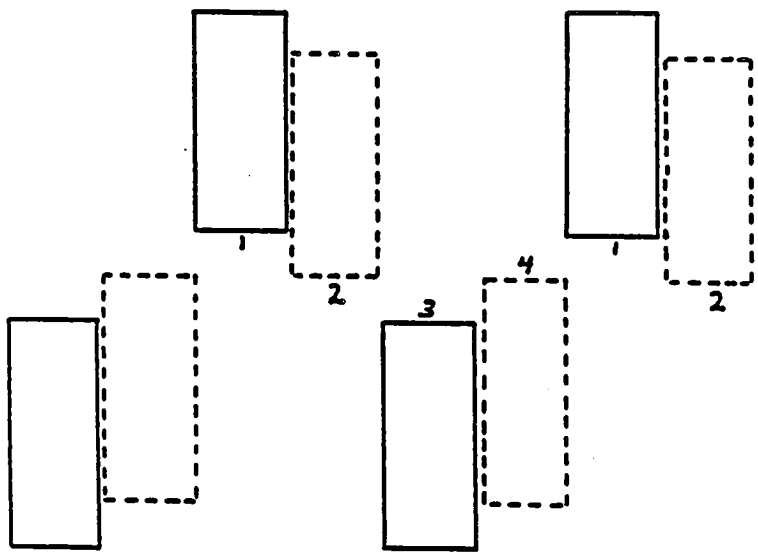
I/O Tracks

Chip V included input/output tracks which require bubble propagation parallel and perpendicular to the applied current direction. Bubble propagation in the storage loop and the I/O tracks perpendicular to the drive current was easily accomplished with a current density of 1.0 to 1.5 ma/μm (larger current densities were not evaluated). Parallel propagation, as depicted in Figure 3.8.10a, was marginal at 1.5 ma/μm. Ejection of the bubbles from the track was the most common failure. It was often observed that a bubble in transit from position 2 would jump to position 3a rather than position 3. Due to the spacing of the apertures, the current density at position 3a is greater than that at position 3, and results in a larger pole strength at 3a. Even though the distance from 2 to 3a is larger than from 2 to 3, the net attraction to 3a is often great enough to cause the bubble to jump from position 2 to 3a.




(a)

I




(b)

Aperture geometries for bubble propagation parallel to the current flow.

Figure 3.8.10

The performance of this style of propagation track could be improved by incorporating the design of Figure 3.8.10b. By increasing the length of the apertures, and also staggering their position, the offending poles are placed further from the intended bubble track and the current density along the track is improved [ 2]. Propagation in the reversed direction should suffer due to these modifications. The staggered aperture arrangement was included in the design of chip VI.

It should be noted that good propagation was also observed in an isolated I/O track when the area around the track was filled with bubbles. These bubbles acted as a barrier, and promoted bubble propagation along the track. As a result of these tests, barriers milled into the garnet were included in chip VII.

Generators

Bubble generation with hairpin type conductors was demonstrated with chip V. Approximately 200 ma of current, one microsecond in duration, was required in a generator with 10 micron wide legs and gap, and 130 ma for 6 micron wide legs and gap. Propagation of just-generated bubbles away from the generator was accomplished for generators placed on I/O tracks running perpendicular to the current flow direction. The high currents involved make routing of the lead in conductors for the generators important to avoid disruption of the nearby bubbles.

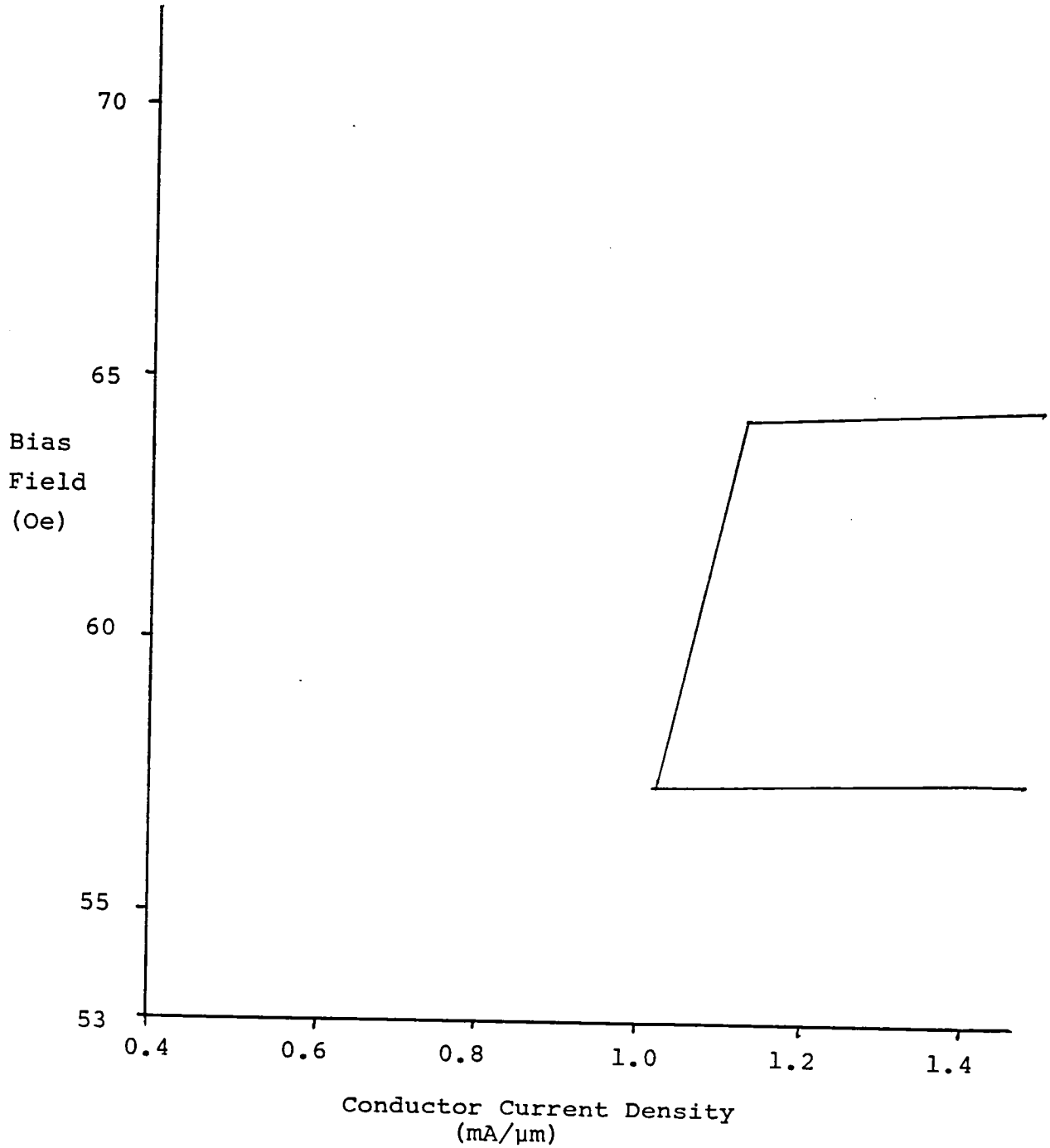
Gates

All three of the merge gates displayed proper operation with bubbles propagated by 5 μs wide current pulses, at a current density in the conductors of 1.5 ma/μm. The current pulses were not overlapping. This represents a more stringent test than that to be used at normal high-speed operation with overlapping pulses.

The sequence control transfer gates incorporate a set of nested apertures at the loop end, and performs the bubble transfer function with a modified propagation pulse sequence, as described in section 2.3.6 of this report. Operating margins were measured for gate 4 in Figure 3.8.5 with non-overlapping 5 μsec wide propagation pulses in the two apertured conductors, and are illustrated in Figure 3.8.11. The lower bias field margin is again determined by bubble strip-out, and the upper margin by bubble collapse. Data at larger values of the conductor current was not taken due to a limitation of the drivers. The same sequence controlled transfer gate was evaluated with bursts of 6 μsec

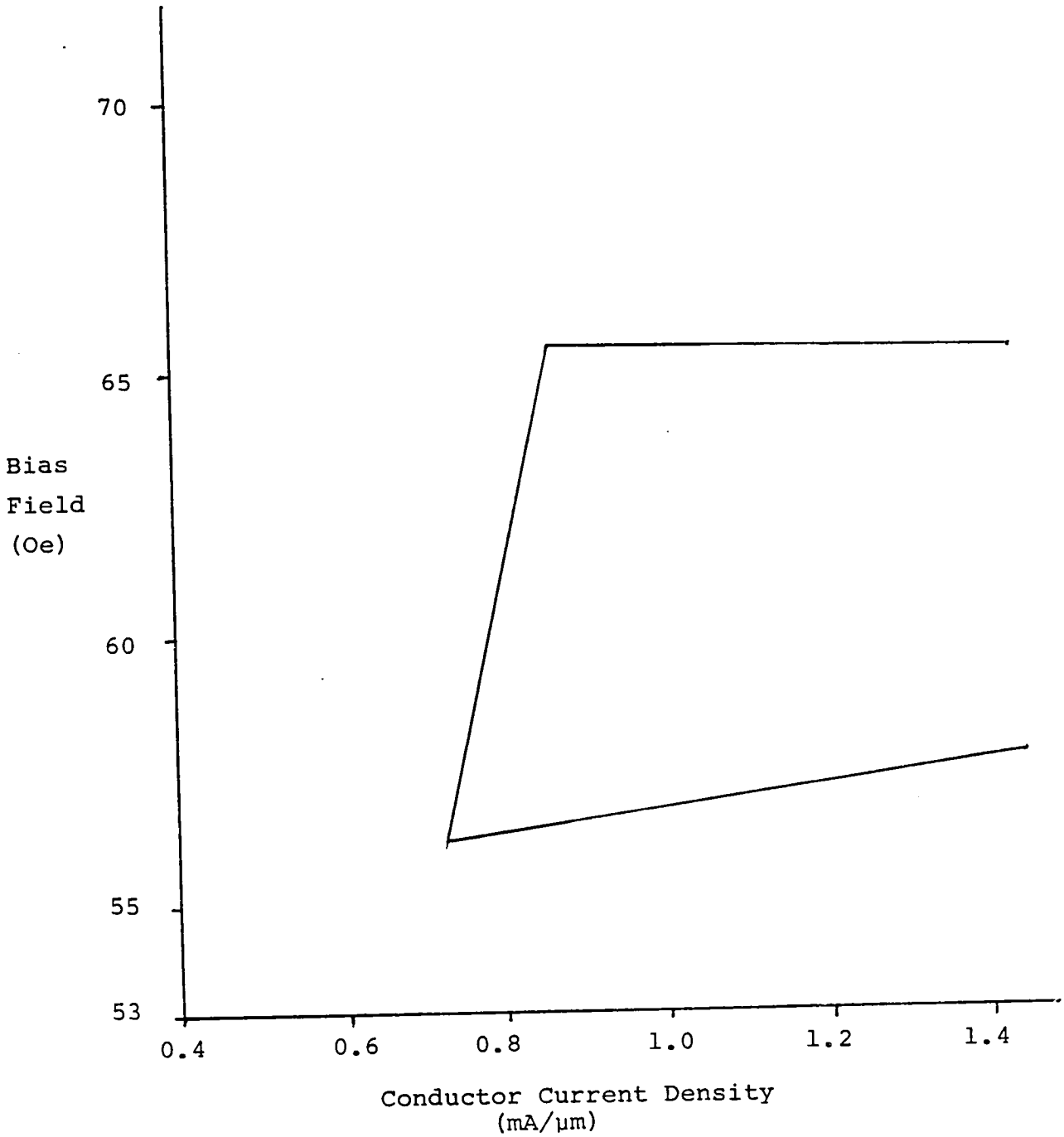
wide pulses with 33% overlap. Figure 3.8.12 shows improved operating margins when compared to the non-overlapping performance.

The hairpin transfer gate (gate 13 in Figure 3.8.5 and Figure 3.3.20) demonstrated proper behavior as it transferred isolated bubbles into and out of the storage loop. At a bias field of 60 Oe, a 25 mA pulse was required to consistently transfer bubbles. Lower currents were able to transfer bubbles at lower bias fields.




Margins for bubble transfer with 5μs non-overlapping pulses using the nested aperture sequence control transfer gate.

Figure 3.8.11




Margins for bubble transfer with 5μs overlapping pulses using the nested aperture sequence control transfer gate.

Figure 3.8.12

## 3.9 Chip VI: Evolution of Chip V I/O Tracks and Gates, Detection

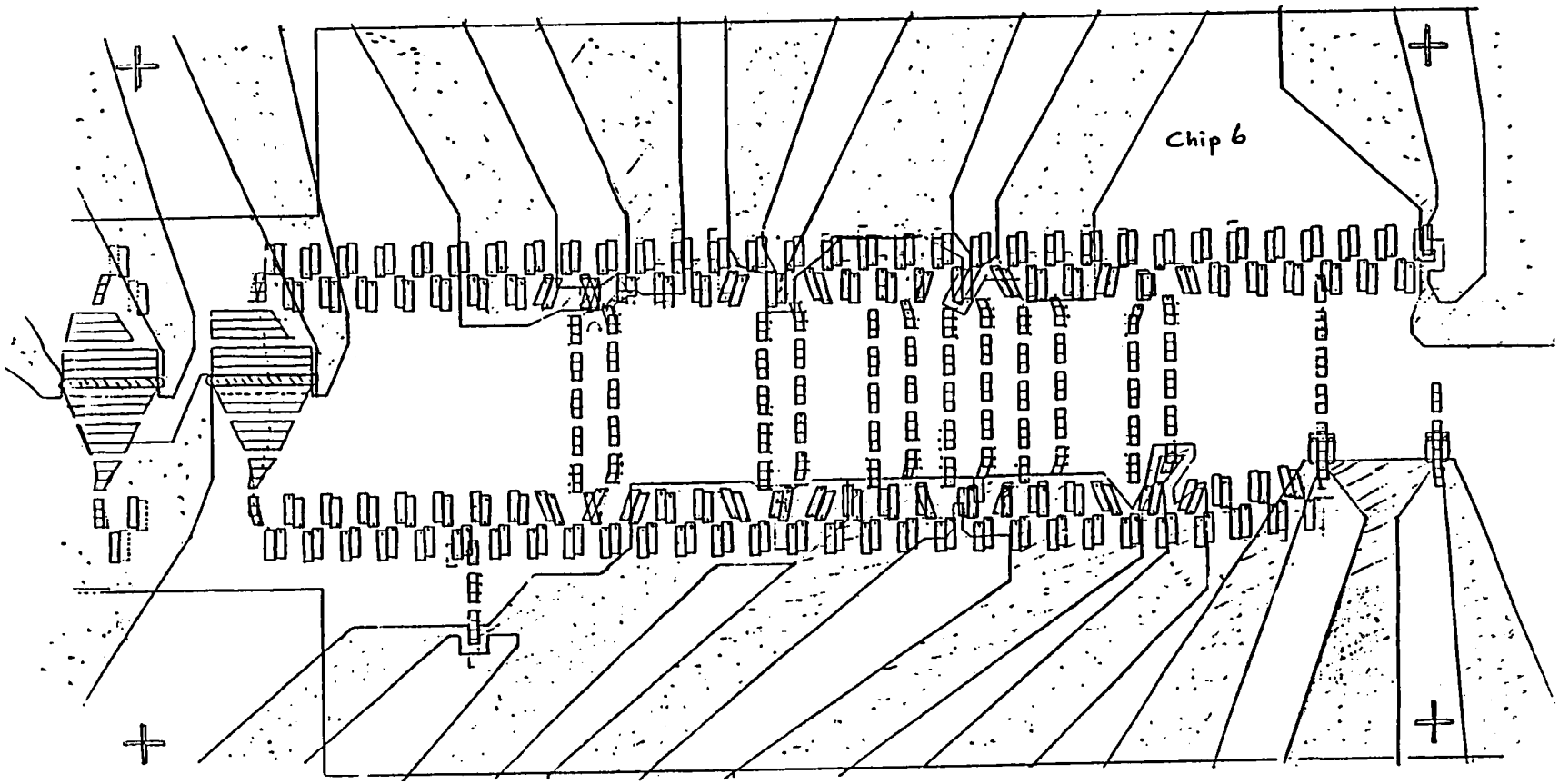
### 3.9.1 Chip VI Description:

Chip VI was designed primarily to test many of the chip V features which were not able to be tested because the chip V I/O track worked so poorly. As a result of chip V tests and at the suggestion of the literature [ 2 ] various aperture offset techniques were studied using apertures cut in conductive paper. For various geometries equi-potential lines were experimentally obtained. From this data the current flow and resulting pole strength can be determined. This technique was used not only for the open sections of the I/O track, but also for the gate regions where a minor loop and the I/O track meet. The resulting chip VI layout is shown in Figure 3.9.1. A schematic layout with identification of key features is given in Figure 3.9.2.

Chip VI includes two hairpin bubble generators, two magneto-resistive detectors, two input/output (I/O) tracks, six minor loops, four with gates at their ends, a swap gate, three different transfer gate designs, two bubble replicate gates, and two merge gates. All of the elements required for a memory device are included in chip VI except for barriers. It is noted here that due to an error in the photomask production process, the aperture in the aperture-controlled transfer gate (Figure 3.9.2) was left out. Therefore this gate was not tested in this work.

Additional dummy apertures were placed in the drive conductor sheets to assure a uniform current density across the width of the sheet. These apertures are not shown in Figure 3.9.1. These dummy apertures, which are not directly involved in bubble propagation, were placed both between and outside of the I/O tracks. These would not be used in a complete memory chip as a fully-populated storage area would also promote a uniform current density.

Two types of bubble detectors were included in the chip VI design (see Section 2.3.9 of this report). A strip-out detector using long apertures was placed at one end of chip VI. The drive conductor sheets were reduced to one-half of their normal width (250 microns rather than 500 microns) in the strip-out detector region to increase the current density. The nominal 35 nm thick permalloy strips in these detectors were 6 microns wide and 75 microns long. One of the strip-out detectors was placed between the two I/O tracks. An identical detector was placed nearby but not in the I/O track bubble path so that it could be used for noise cancellation in a bridge detector circuit.

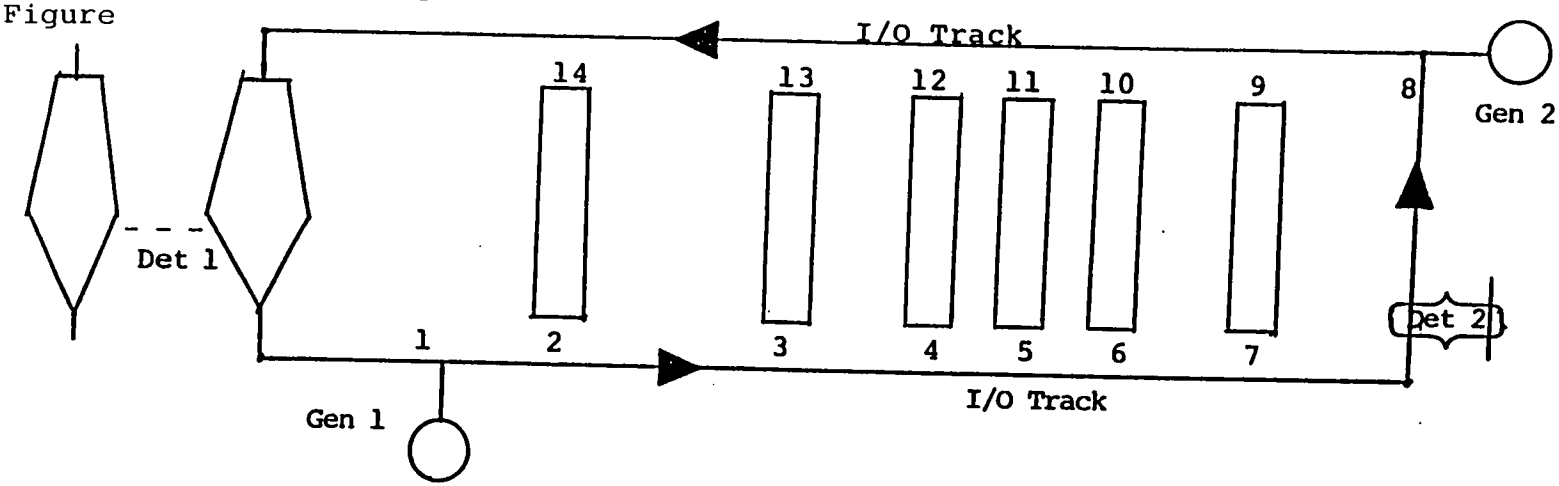



Chip VI geometry including the control conductors.

Figure 3.9.1

Figure

Chip 6 Layout




Gen 1 - hairpin generator
Gen 2 - hairpin generator
Det 1 - strip-out detector (incl. dummy for noise cancellation)
Det 2 - non-strip-out detector (incl. dummy for noise cancellation)
1 - merge gate
2 - phase matching corner turn for minor loop
3 - aperture controlled transfer gate
4 - minor loop end - no gate
5 - N transfer gate
6 - minor loop end - no gate
7 - hairpin replicate gate
8 - merge gate
9 - sequence controlled transfer gate
10 - minor loop end - no gate
11 - hairpin replicate gate (designed for use with ion-impant area)
12 - minor loop end - no gate
13 - hairpin transfer gate
14 - control conductor swap gate

Schematic layout for Chip VI circuit.

Figure 3.9.2

The non-stripout detector was included in chip VI at the end opposite to the strip-out detector. In this design the bubble moves between two short permalloy elements (20 microns long by 6 microns wide). This non-strip-out design was developed to:

1. Eliminate the need for stripping out which is mobility limited. If one is moving the bubbles at or near the material limit, then a rapid strip-out device (as used in some conventional designs) cannot be used.

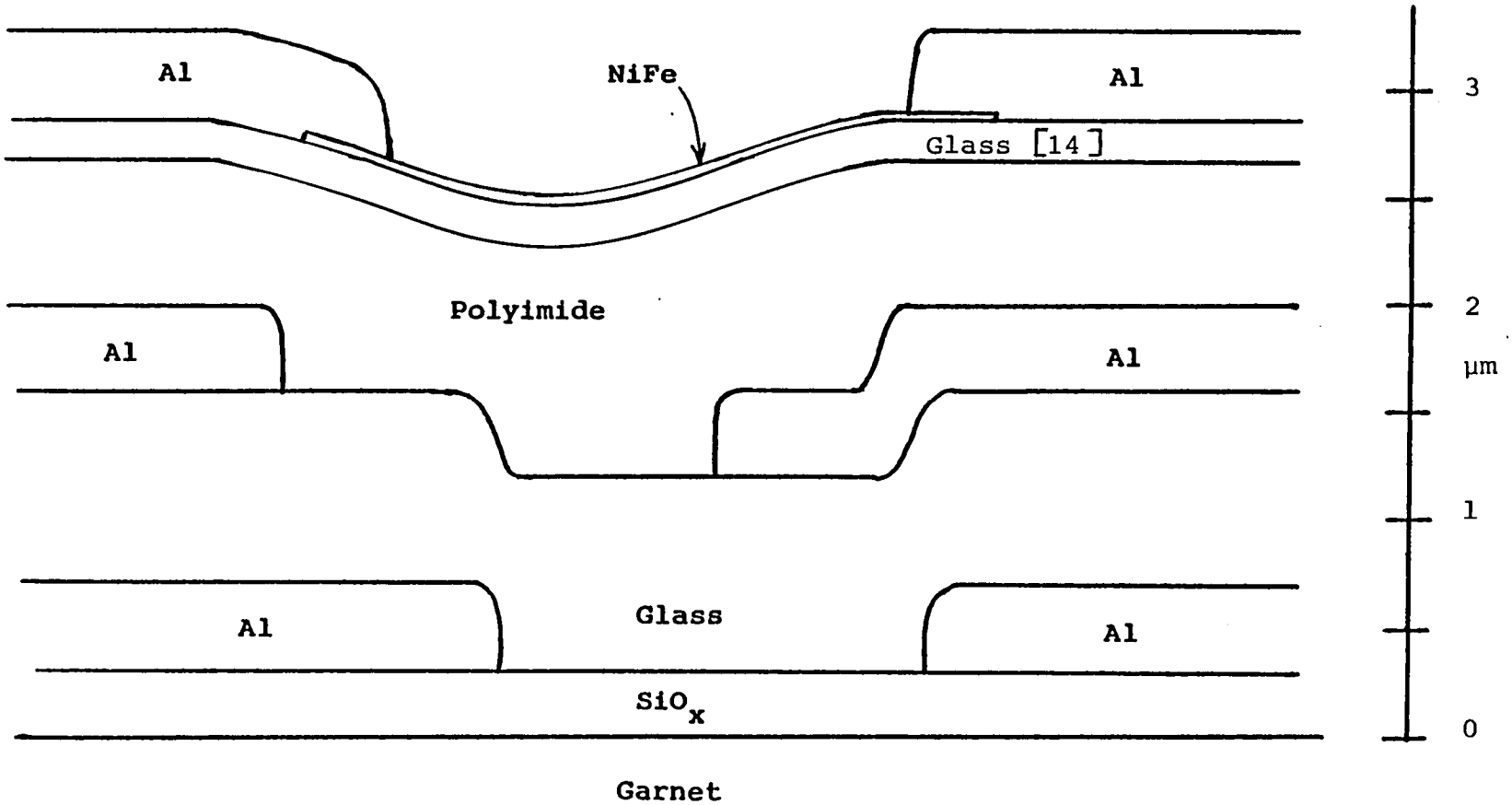
2. Use less chip real estate.

3. Eliminate the need for higher drive sheet currents in the vicinity of the detector (these are required for the stripping out to occur).

4. Take advantage of the thin film, optimally in-plane magnetically biased Ni-Fe which can be used in these devices.

### 3.9.2 Fabrication

The first set of chip VI circuits used 7059 glass as the only insulator material between the two aluminum (apertured) drive layers and also as the insulator between the top drive layer and the third conducting layer (which included the control conductors and the permalloy detector(s). Some difficulty with rough aluminum deposition and the difficulty of the thin (35 nm) permalloy to cover the milled aluminum apertures initiated a study to planarize the circuit (this would also be very helpful in chip VII where milled barriers would be present). A description of this planarizing work is included elsewhere in this report (Appendix A). The final set of chip VI samples produced used a polyimide planarizing layer as well as thicker than usual insulating layers (see Figure 3.9.3). The thicker insulating layers were used to avoid electrical shorts which developed at some of the aperture edges in some earlier samples. Thinner insulating layers which are electrically adequate will be necessary to scale devices to the 2 micron bubble size.




Schematic cross section of Chip VI

Figure 3.9.3

Ni-Fe Detector Fabrication:

The resistance characteristic (magnetoresistance) is expressed as a percentage, based on the resistivity difference between the orthogonal magnetization states ($\rho_{max.}-\rho_{min.}$), divided by the maximum resistivity, $\rho_{max.}$. This is commonly expressed as $\Delta\rho/\rho$ but, by definition, a constant dimensional factor, film length ÷ (width x thickness), relates resistance R to resistivity $\rho$, so one may consider either $\Delta R/R$ or $\Delta\rho/\rho$. The percentages are the same in either case. The Ni-Fe films used in these studies had $\Delta R/R$ values typically between 2 and 2.8% as measured on $Si_3N_4$ or $SiO_2$-coated Si wafer test samples using a constant current four-probe bridge device and a permanent magnet. These saturation values were not necessarily achieved in the etched sensors due to geometry effects and resulting non-ideal domain formations.

Deposition parameters of importance to the magnetic properties of the film include composition, deposition temperature, thickness, and substrate material and structure. The as-deposited properties are further influenced by geometrical effects from etching the sensor element, such as shape anisotropy (tending to orient the magnetization in a particular direction) and demagnetizing field which opposes any applied fields. Also, subsequent film layers and heat cycling can influence the magnetic film properties.

All of the sensor films used in these studies were physical-vapor-deposited from an alumina crucible by heating with RF induction. Initial melt composition was 82.8% nickel, 17.2% iron with a small additive of pure nickel for fine tuning of magnetostriction to a near-zero value. Substrate temperature during deposition was nominally 250°, and deposition rate was 10Å/second. A magnetic orienting field of ~95 gauss was applied during most of the depositions, so that it and the shape anisotropy fields of the subsequently ion-etched sensor strips established the easy axes of magnetization. Thickness was generally ~350Å in keeping with published data for maximum magnetoresistance values [ 7 ]. Our experiments with higher deposition temperatures and greater thickness indicated that improvements may be possible. Sensor element dimensions were approximately 6µm x 25µm and 6µm x 80µm, with some loss in current path length due to end contacts.

Hysteresis loop measurements of 8 mm dia. test films deposited on borosilicate glass substrates at 250°C showed typical values of coercive force, $H_c$, to be ~2.0 oersteds

and anisotropy field, $H_k$, to be ~3.5 oersteds when deposited in the presence of a 95 oersted orienting field. Actual values of $H_c$ and $H_k$ in the small sensor strips are not readily measurable, but underlying surface roughness, such as was encountered when aluminum was one of the underlayers, is known to cause significant local and general changes in these properties.

Polyimide serves as an excellent conformal, smoothing coating. Ni-Fe test films deposited on 2000Å of $SiO_2$ over fully cured PI had $H_c$ & $H_k$ values similar to films deposited on glass. Polyimide does absorb water, however, which could outgas during Ni-Fe deposition. As a precaution, devices incorporating polyimide were stored in a desiccator between process steps.

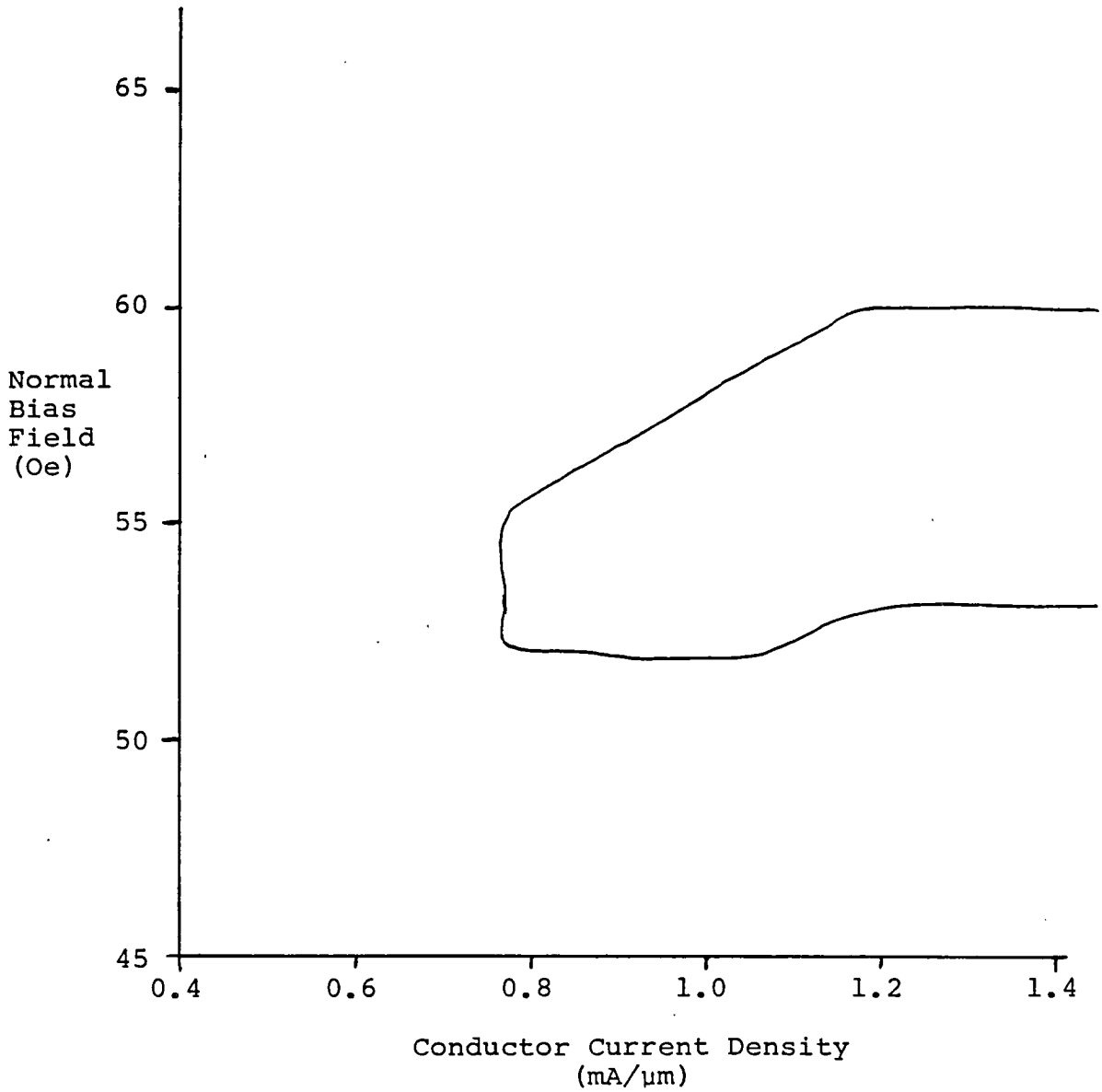
### 3.9.3 Testing

Propagation

Chip VI showed for the first time in this study an I/O track which moved bubbles successfully. Propagation margins for Chip VI were obtained for overlapping and non-overlapping 5 microsecond pulses in the aluminum drive layers. When overlapping pulses were used a 33% (or 1.6 microsecond) overlap of the pulses was used. Current densities up to 1.4 mA/micron were allowed by the drive electronics. Operating margins for a chip VI I/O track and a minor loop are given in Figures 3.9.4 and 3.9.5. These margins do not reflect occasional bubble propagation failures where an I/O track and a storage loop meet. These failures included:

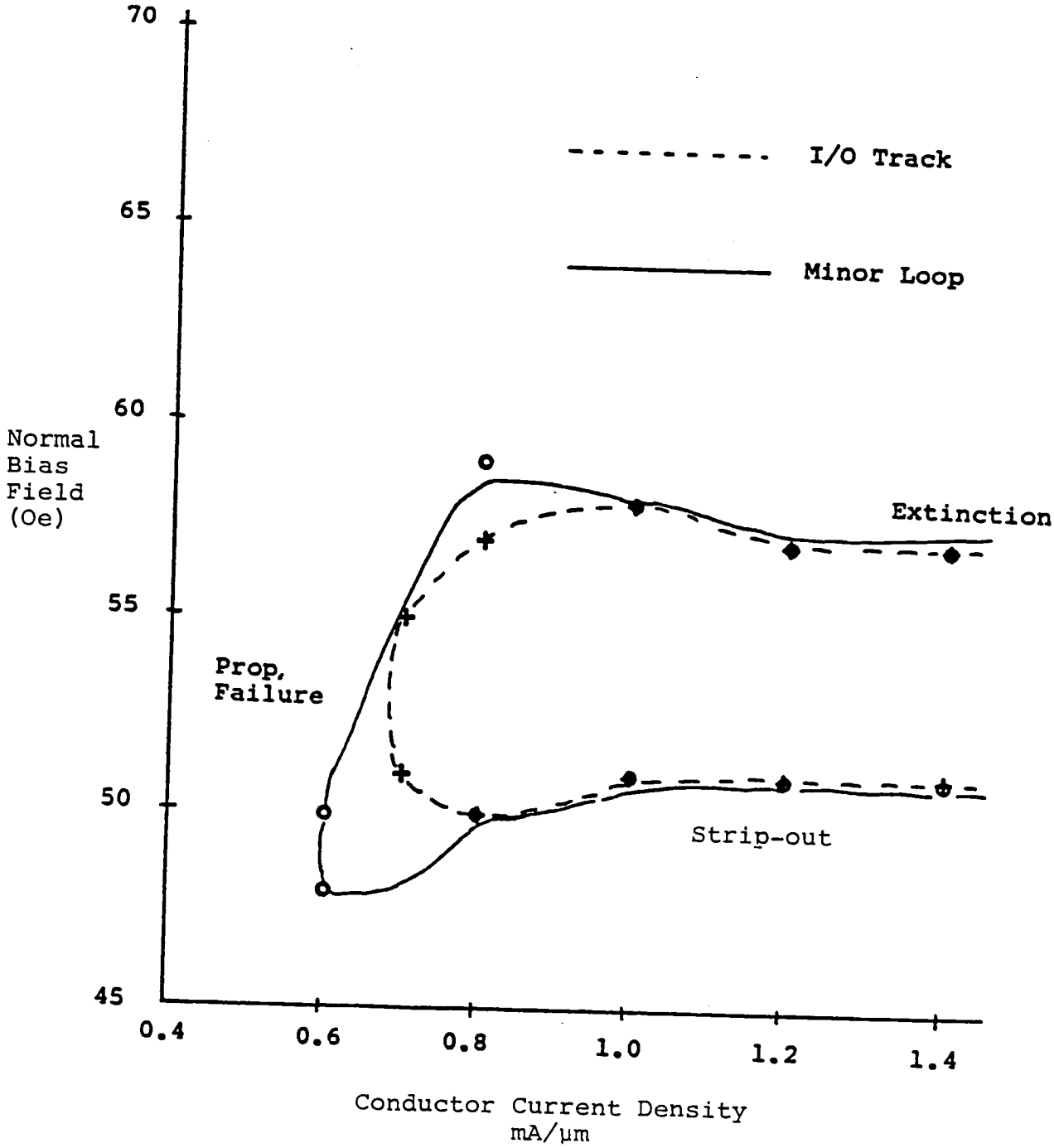
1. Bubble movement from I/O track to minor loop (and vice versa) with no gate pulses. This motion appeared to be occurring at random about 10% at the time. All samples showed similar behavior in this regard. Detailed studies of this failure were not carried out. Design of future gate architectures shall need to optimize gate geometry and/or use barriers to eliminate this problem. Chip VII successfully used barriers to prevent this failure.

2. Bubbles in the I/O track were occasionally pulled to the wrong end of the I/O track apertures or would oscillate between an aperture's inner and outer ends. Refer to the milled barrier discussion for Chip VII (Section 3.10 of this report) to see the effects of barriers in preventing both of these propagation problems.




Operating margins for typical Chip VI minor loop using 5µs non-overlapping pulses.

Figure 3.9.4




Operating margins for typical Chip VI I/O tracks and minor loops using 5μs overlapping pulses in bursts of four.

Figure 3.9.5

One of the test limitations for this device was the requirement that testing be done on isolated bubbles or on small sets of bubbles isolated from all others for any of the high speed tests. This was due to the absence of a data coding scheme in this phase of the project. While some very slow propagation testing was possible with visual observation "detecting" the bubbles "in motion," high speed tests with overlapping pulses could only show initial and final bubble positions and not the exact path of a given bubble.

Detectors

The stripout detectors underwent two types of tests. The first was with bursts of overlapping 100 ms pulses where stripping-out was observed visually. The effects of high speed pulses (e.g. 5 microsecond) could not be studied with the television camera-microscope system available or with the operator's eyes available.

The second type of test involved using the magnetoresistive permalloy stripes as they would be used in a device-measuring resistance change as a function of a bubble presence or bubble non-presence. The initial results of this work were disappointing with the signal level approximately equal to the noise level. The signal level was typically 250 microvolts for a 5 mA current through the active detector. The noise included the resistance changes related to the somewhat random variations of the domain structure of the permalloy.

A study of domain structures in both short and long permalloy stripes was initiated to attempt to understand the domain instabilities observed. It was found that the 35 nm permalloy was showing the buckling domain structures recently reporting in the literature [ 8 ]. The details of the buckled domains were sensitive to the 6 - 10 G fields due to the drive pulses in the device. Unfortunately the behavior was not consistent. Therefore the use of a dummy detector to cancel common noise was not able to help in this case.

It is now known that the application of an in-plane bias field would be helpful in increasing the signal level. See the chip VII detector section of this report for some work with in-plane biasing and the resultant higher signal levels.

The non-strip-out detectors showed the same type of buckling behavior as the longer permalloy strips of the strip-out detectors. Signal levels of 500 μV were just barely above

the random noise produced by the permalloy domain structure shifts. Again, refer to the chip VII detector section for more successful results using this detector approach.

Generators

Two hairpin generators were included in the chip VI design (refer to Figures 3.9.1 and 3.9.2). The physical dimensions of the two generators were identical. One of the generators was placed on an extension of an I/O track. The other one was placed outside of one of the I/O tracks along a set of drive apertures identical to those of a storage loop.

Both generators produced bubbles with current pulses of 120 mA and above with 5 microsecond pulses. The generator located outside of the I/O track (Gen 1 in Figure 3.9.2) produced bubbles and the drive apertures moved these bubbles in a very controlled fashion to the I/O track where they merged with and moved along the I/O track. The generator positioned on the extended I/O track produced bubbles as expected, but the I/O track did not propagate these bubbles. It was determined that this failure to propagate occurred because the I/O track began at the center of the hairpin and not behind the hairpin. The repulsion of the end of a (missing) aperture is required to get the bubble started along the track.

Gate Testing

The following is a review of the chip VI gate testing which was accomplished. It should be noted that gate testing on chip VI and VII suffered from two problems. The first were delays in fabricating working circuits to test. Time was not available under this contract to do thorough testing of all gates. The second problem were delays in delivery of capital equipment and supplies to construct test equipment. Thus the following review of chip VI gate tests is necessarily brief. Additional testing is expected to continue under Sperry funding after the completion of this report.

The control conductor swap gate (gate 14 in Figure 3.9.2 and Figure 2.3.26) was tested as a one-way transfer gate (one half of the swap) with single polarity gate pulses. Pulses of 500 ns at 17 mA were effective in transferring bubbles in either direction. These tests were done with isolated bubbles and with groups of bubbles with a spacing to diameter ratio of $\sim$3.5. At this spacing the bubbles interact but are not so close that they must be present at all sites to prevent movement of bubbles to neighboring empty sites by bubble interaction only. The spatial separation of the two bubble paths in this gate and the

successful operation of each half of the gate provide encouragement that this gate will properly swap bubbles when tested with a bipolar drive. Parts for the construction of the driver arrived during the writing of this report. Further studies will be required to evaluate the bubble swapping function of this gate as well as the behavior of this gate with a full array of closely-spaced bubbles.

The design and operation of the sequence controlled transfer gate is provided in Section 2.3.8. In chip VI this gate design (gate 9 in Figure 3.9.2) was tested with quasi-static 5 μs non-overlapping pulses. As anticipated, changing the propagation sequence from the normal 1,2,3,4 sequence to the 1,2,1,4 sequence causes a bubble to move from the storage loop to the I/O track. Bubbles in the storage loop and the I/O track other than the bubble at the gate position idle in place during the 1,2,1,4 pulse sequence.

Memory Chip Initialization

One solution to the problem of initializing a self-structured bubble memory device has been experimentally demonstrated. Because of the close spacing of bubbles in the self-structured device, bubbles probably can not simply fill the storage area by being propagated in individually as in conventional bubble devices. An approach for generating bubbles at all positions in the storage area simultaneously may be needed. One approach, which was demonstrated earlier was to use a very large pulse in a propagation conductor. This pulse would generate bubbles at all apertures simultaneously and populate the device. The current required, however, was more than an order of magnitude greater than normal propagation current levels. A pulse this size was close to damaging the conductor despite the device being very small and fabricated on low $4\pi M$ garnet material. As such, this approach was not scaleable to larger devices on material with higher $4\pi M$. The present approach is to heat the garnet and device to reduce $4\pi M$ to a lower value and reduce the necessary current for bubble generation. In the present garnet material with a $4\pi M$ of 125 oersted at room temperature, raising the temperature by $\sim 30^{\circ}C$ reduced the bubble generation current to the normal propagation current level. Two techniques were used to heat the garnet; a heat gun and joule heating with currents in the propagation conductors. This approach should be scaleable to larger devices with higher $4\pi M$ values. If the propagation conductor is used for local heating, a device with multiple storage areas could possibly have them individually populated.

## 3.10 Chip VII Design, Fabrication, and Testing

### 3.10.1 Chip VII Description:

Chip VII design efforts centered on adding various types of milled barriers to the chip VI circuit design. Because bubble propagation and initial gate tests on chip VI circuits showed proper behavior, it was decided to use the chip VI masks for chip VII aperture drive conductors and control conductor layers. Additional masks were fabricated to test three barrier designs. They are:

1. Mesa barriers where the I/O tracks and the storage loops are positioned within mesas which are connected at the gates (Figure 3.10.1a).

2. Recess barriers containing the storage loops and the I/O tracks with recess connections through the gate regions (Figure 3.10.1b).

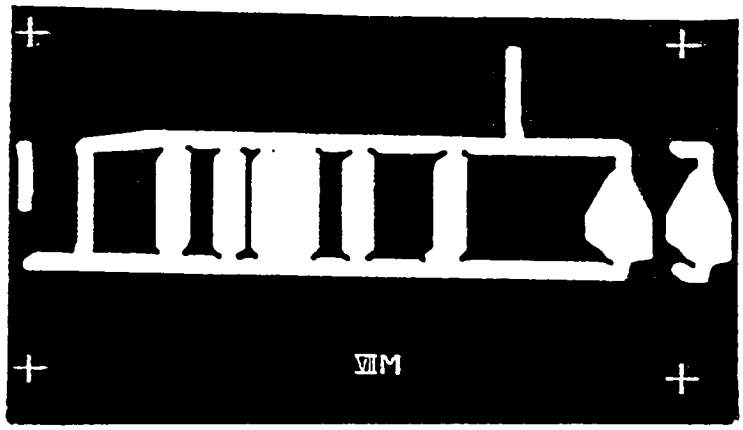
3. Recess barriers containing the storage loops and the I/O tracks with no recess connection at the gates (Figure 3.10.1c).

As noted in more detail in the Fabrication section below, it was decided to evaluate the three chip VII designs with two different orders of construction. One set of samples would have the two aluminum drive layers put down first and the control conductors (and permalloy detectors) put on last (farthest from the garnet). The other set would have the control conductors (and permalloy detectors) put down first (closest to the garnet) with the aluminum conductor drive layers put down above. These variations were designed to test the drive layer effectiveness, gating effects, and detector signal levels as a function of spacing from the magnetic garnet layer.

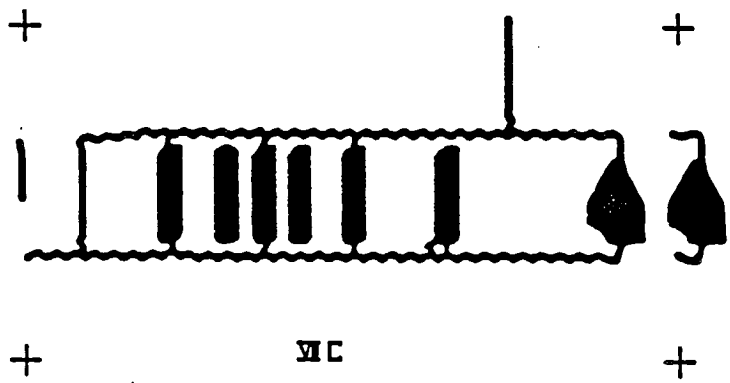
### 3.10.2 Chip VII Fabrication:

Fabrication of five of the planned set of six chips was completed. One of the chips was broken in process and was not replaced due to time constraints. Four circuits were patterned on each chip. Typical useful production yield provided 1 to 4 useable circuits per chip. A listing of the circuits which were completed is given below. The number of circuits of each type is given in parenthesis.

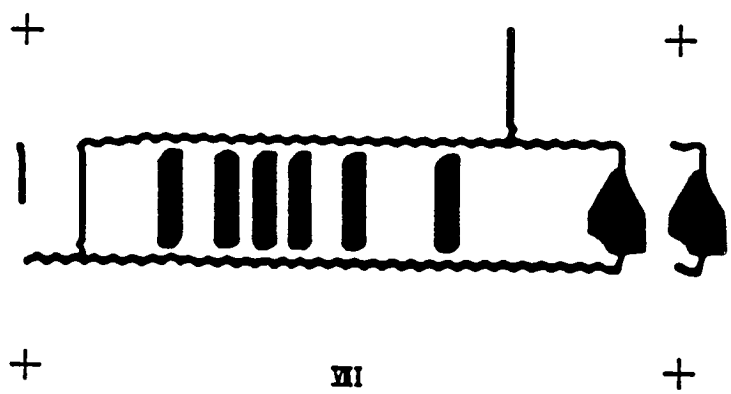
Control conductor and permalloy deposited last:
- (4) connected recess barrier
- (0) non-connected recess barrier
- (4) mesa barrier




(a) Chip VII Mesa Barriers.




(b) Chip VII Recess Barriers, Loops & I/O Tracks Connected.




(c) Chip VII Recess Barriers, Loops & I/O Tracks Isolated.

Figure 3.10.1

Control conductor and permalloy deposited first:
(1) connected recess barrier
(2) non-connected recess barrier
(2) mesa barrier

A polyimide planarizing layer and approximately 200 nm of 7059 glass were put down after the barriers had been milled into the garnet. Subsequent layers of aluminum and 7059 glass were used to complete fabrication. The permalloy for the detectors was deposited just before the aluminum control conductors for each chip. Figure 3.10.2 shows the cross section of one set of chip VII samples with the permalloy and control conductors below the drive conductor layers.

### 3.10.3 Chip VII Testing:

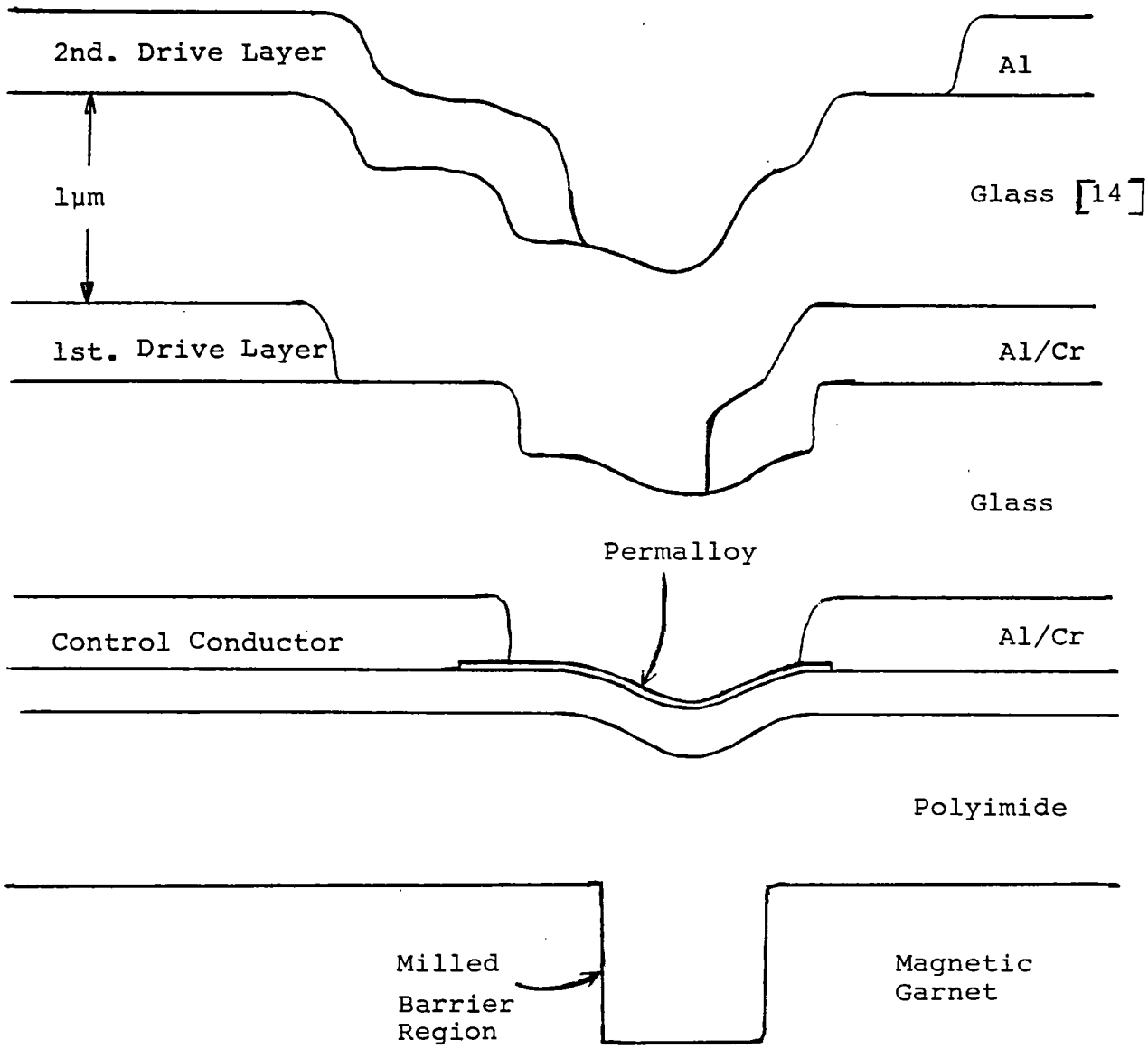
Propagation:

Propagation tests on chip VII circuits has shown that barriers are a valuable aid to device performance. The two propagation failures observed in chip VI,

a) bubbles passing from I/O track to minor loop, and vice versa, with no gate pulses, and

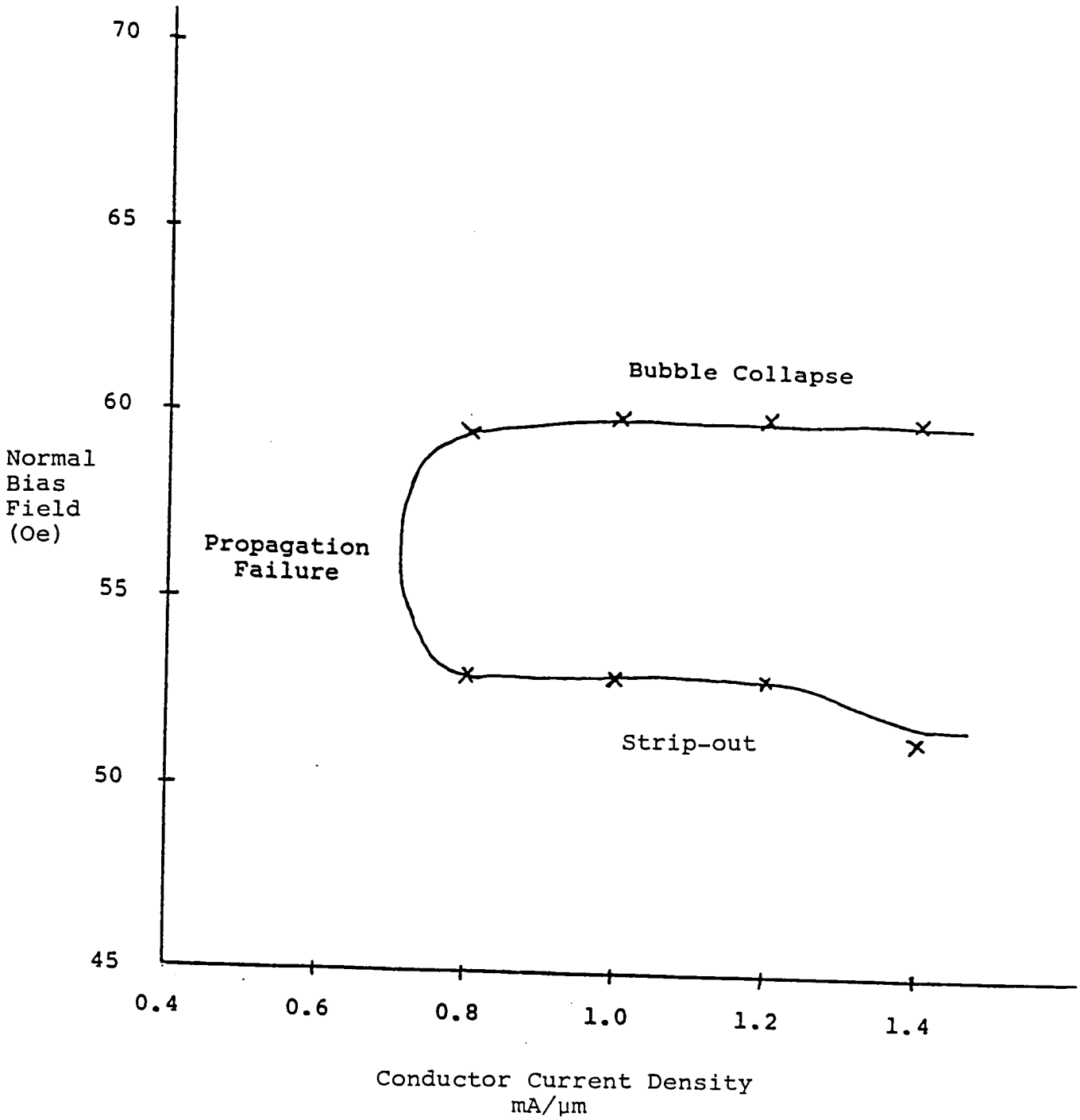
b) bubbles moving to the wrong end of the I/O track apertures (see page 3-49)

were not seen in the non-connected recess barrier circuits studied. The connected recess barrier chips and the mesa barrier chips still showed the occasional interchange of bubbles between the storage loops and the I/O tracks. One new failure mechanism was observed with isolated bubbles and the connected recess barriers. A bubble moving in a storage loop toward an I/O track would hug the barrier as expected. As the bubble reached the end of the storage loop, where the normal bubble path would move it around the end of the storage loop and down the other side, the apertures did not always apply enough force to pull the bubble away from the barrier. The bubble would occasionally stick to the wall or would be pulled into the I/O track. This suggests that non-connected recess barriers would be preferred if appropriate gating structures are used which will pull the bubbles through the barrier. It is not yet clear what effect self-structuring will have on these types of problems. A fully populated system cannot be studied without either a data coding system or a high speed microphotographic system. Figures 3.10.3 through 3.10.4 give operating margins for storage loops and I/O tracks for chip VII samples studied.



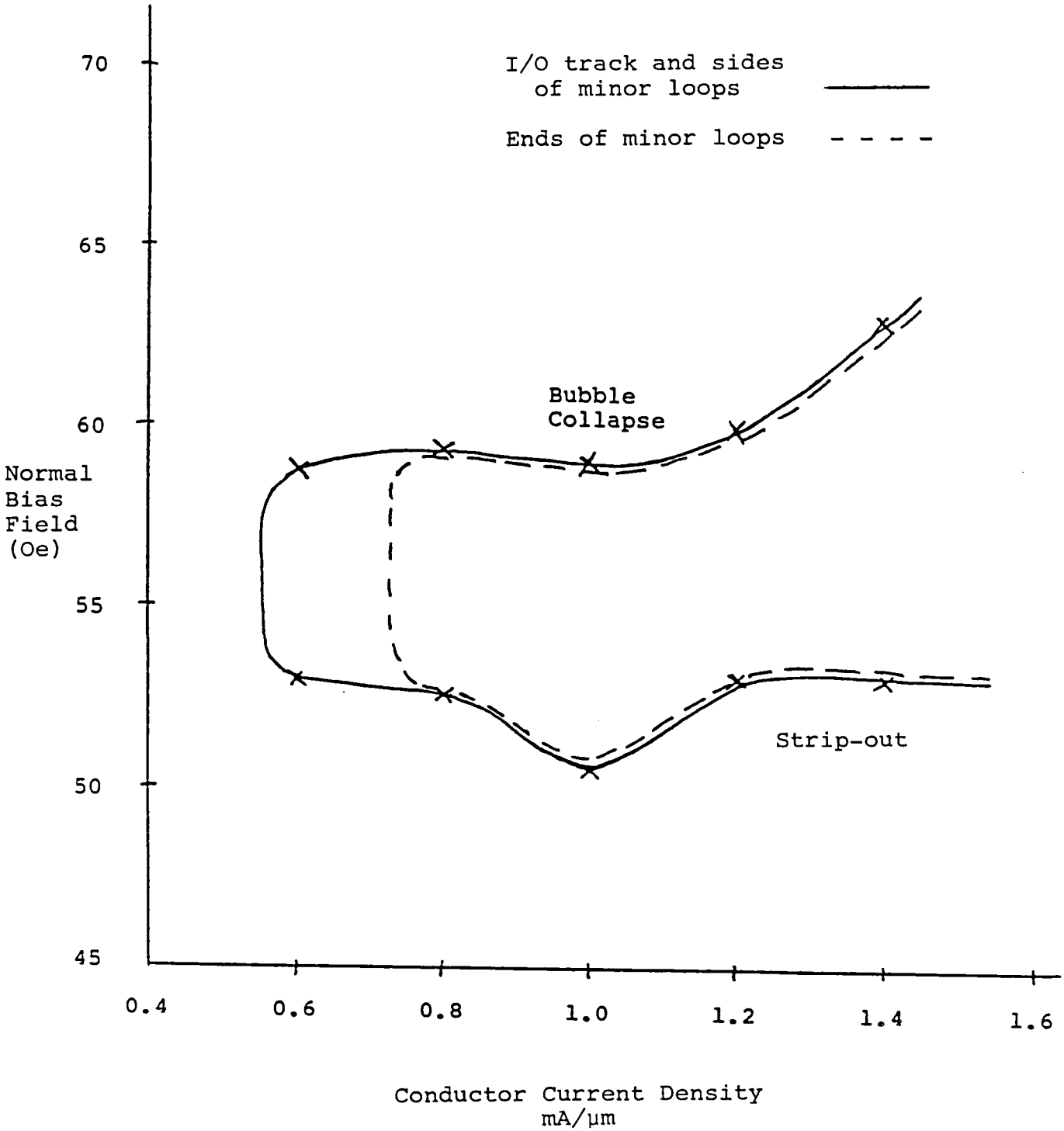

Schematic cross section of Chip VII circuits with permalloy and control conductors below propagation conductors. Vertical and horizontal scales are not the same.

Figure 3.10.2




Operating margins I/O track and sides of minor loops for Chip VII sample 7473 with connected recess barriers using 5μs non-overlapping pulses in bursts of four.

Figure 3.10.3




Operating margins for Chip VII sample 7473 with connected recess barriers using 5μs overlapping pulses in bursts of four.

Figure 3.10.4

Detectors

The primary detector work with the chip VII samples was to study the effect of having the thin permalloy detector elements close to the magnetic garnet as compared with the permalloy detectors on top of the drive conductor layers. The first observation of the permalloy first samples showed that the permalloy-bubble interaction was strong enough to trap the bubbles adjacent to (or partially under) the permalloy for an isolated bubble. In most cases a series of bubbles would propagate through the detectors (due to self-structuring), although in some samples the permalloy-bubble interaction was so strong that only occasionally would a bubble escape from the permalloy even with a bubble pushing from behind. In this case the bubbles would stack up in the I/O track behind the detector. The polyimide and 7059 glass spacer layer was nominally one micron thick for these samples (see Figure 3.10.2). Variations in this thickness or variations in the permalloy may explain the subtle differences in bubble trapping observed in these films. It should be noted that the bubbles (nominal 5 to 6 micron diameter) were moving in 6 micron thick magnetic garnet (or nominally 5 micron thick where the garnet had been milled). The series of chip VII samples studied had milling depths of 0.75 micron and 1.1 micron.

The much stronger permalloy-bubbles interaction also increased the signal level (change in detector resistance). However, the domain buckling effect was still keeping the noise close to the signal level. When a 38 G external in-plane field was applied perpendicular to the long axis of the short permalloy elements (non-stripping detector), the detector signal became much stronger with a typical signal change of 1 mV with a 5 mA constant dc current through the detector when a bubble came into the detector. A 15 mA current through the detector gave a 3 mV signal. These results are very encouraging.

The only tests performed on the stripout detectors with the permalloy close to the garnet was a quasistatic study of the effects of stripping a bubble out along one of the permalloy elements. An isolated bubble was propagated until it was next to the long permalloy element of the strip-out detector. Due to the bubble-permalloy interaction, the bubble tends to stay immediately adjacent to the permalloy. The normal bias field is now reduced. The bubble strips out along the permalloy. As the strip is lengthened and shortened (to a bubble) the voltage change across the

permalloy is measured for a constant current through the detector. For a 5 mA current in the permalloy a 3.5 mV signal was observed with no in-plane biasing field. This is nearly an order of magnitude above the noise level in these long detector elements.

Gate Operation with Barriers

The replicate gate (gate 7 in Figure 3.9.2) with the non-connected recess barrier (Figure 3.10.1c) was studied to attempt to determine this gate's ability to strip out a bubble through the milled barrier. Observations were made using the microscope-television system and are summarized below.

Quasi-static experiments using 100 ms pulses in the replicate gate were used to strip out bubbles with no propagation pulses. The bubbles were initially inside of the gate conductor in either the milled storage loop area or the milled I/O track. For most bubbles a 20 mA current amplitude was sufficient to cause stripping out to occur in the milled area. This amplitude would not cause stripping out to penetrate into the barrier region. A 30 mA current amplitude was sufficient to strip the bubble out and to punch it through the barrier. There were variations in the absolute values of these currents for different bubbles (this may be an indication of the presence of hard and soft bubbles), but the ratio between strip-out only and strip-out with barrier punch through remained 2:3 within the uncertainties of the measurements.

This confirms experimentally that with a power penalty, gates should be able to move bubbles across a barrier separating the storage and I/O track areas. This is desirable for preventing the propagation failures noted at the beginning of this section and also because it permits the I/O tracks to be unpopulated or non-self-structured if desired.

## 4.0 Device Architecture Design

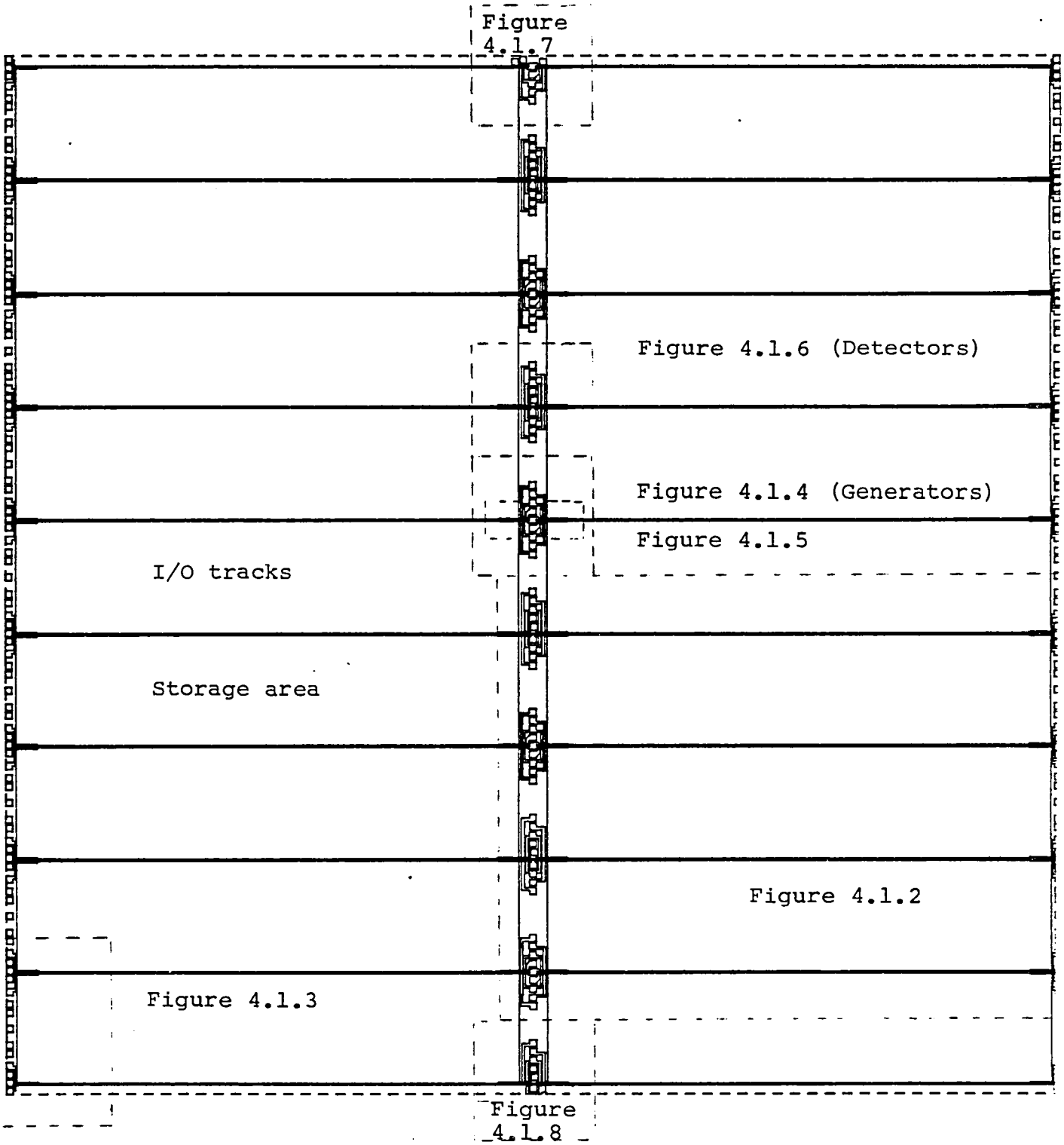
Section 4.1 describes two variations each of two device architecture designs which are based on the components covered in section 3. Both designs meet the NASA goals of 10 megabit capacity, 1.5 megahertz data rate, 1.5 x 1.5 centimeter square die and 2 micron lithography minimum feature size. One design, in addition, meets the remaining NASA device goal of 18 separate storage areas of which two are redundant for fabrication yield purposes. The other design is an 8 storage area device which was developed on Sperry IR&D funding. The two variations of each design comprise a high bonding pad count version and a lower bonding pad count version. The high count versions assume independent connections for each end of every conductor in the chip. This would not be a likely method of constructing a device, however, it makes the placement of the individual components and their required connection easier to interpret in the black and white plots of this report. The low pad count versions make some attempt to reasonably connect conductors to common bonding connections. Black and white plots of these versions are easily interpreted in conjunction with the high pad count plots.

In the literature there has been concern over power dissipation levels for current accessed bubble chip designs [15, 16]. Therefore section 4.2 has been included to model power and thermal results for the 18 storage area design. The overall results are that both power dissipation and current densities in the various conductors are within usable range. Two different operating modes were used in the modeling; a tape recorder equivalent where data is read or written in sequential blocks, and a worst case random block access mode where the next block always requires a complete cycling of the storage loops. Section 4.3 summarizes the significant aspects of all designs and makes recommendations regarding tradeoffs demonstrated by differences between them. Packaging and footprint expectations are also discussed. Finally, a "what next" discussion covers briefly the additional tasks needed to achieve a proof of concept chip.

## 4.1 Physical Layout and Discussion

18 Storage Region Device-High Pad Count Version: Physical Description.

Figure 4.1.1 shows an overall view of this design where the general placement of the storage areas, I/O tracks, generators, and detectors can be seen. In addition, the figure outlines the regions displayed in Figures 4.1.2 through 4.1.8. Approximately 92% of the die area is used for bubble storage area. After excluding two redundant regions, the effective storage area comprises 82% of the die. The storage areas are made up of loops where bubbles are propagated in slipping columns in directions normal to the current flow directions.




18 storage region device-high pad count version. Overall architecture is shown as well as the areas illustrated in Figures 4.1.2 - 4.1.8

Figure 4.1.1

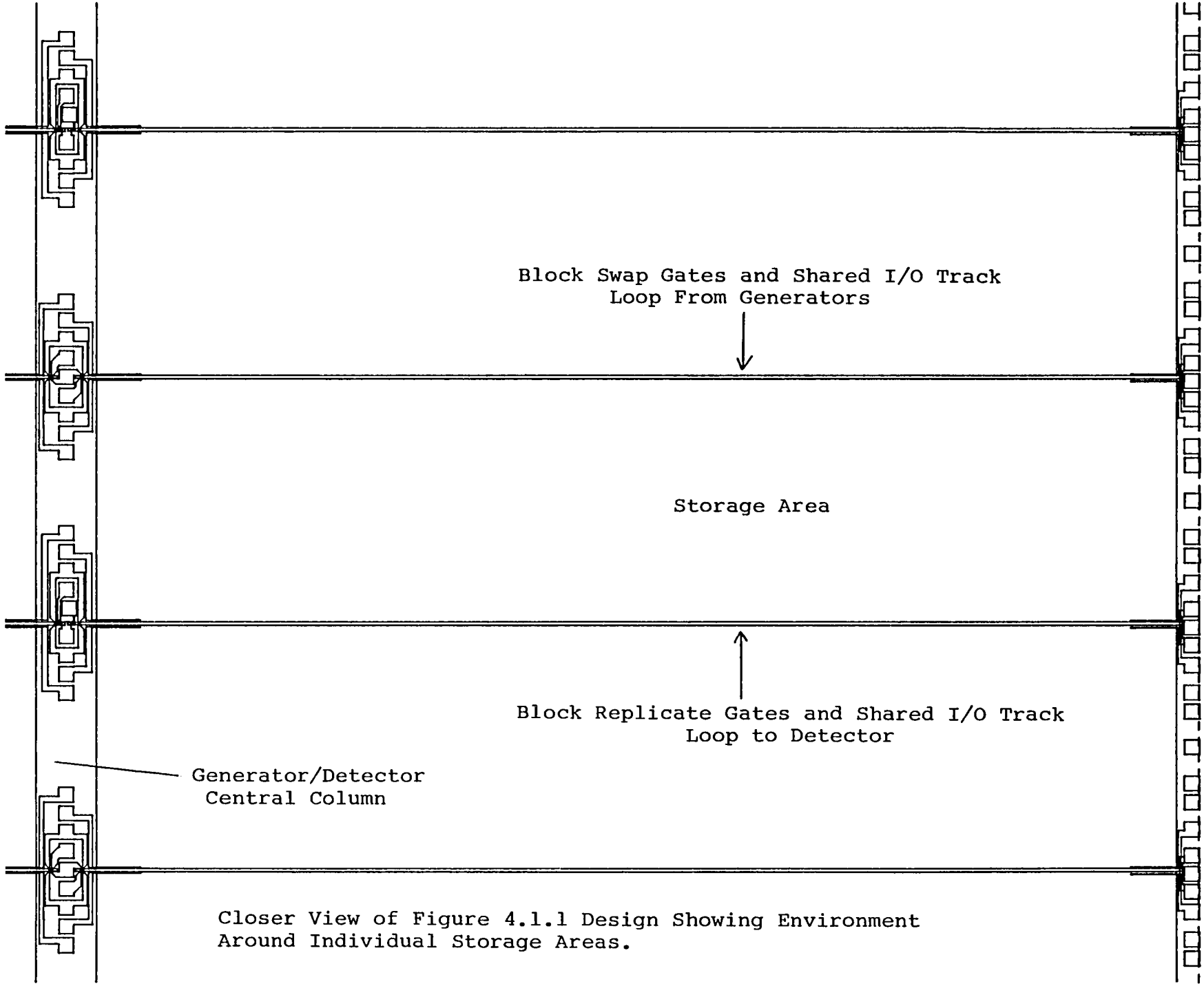
As shown in Figure 4.1.1, the device has a column of generators and detectors in the middle of the chip and has nine storage areas on either side of this column. Each storage area has an I/O track on either side of it. On one side is an I/O track which uses block replication to copy data out for reading. On the other side of the storage area, block swapping moves written data from the I/O track into the storage areas.

Figure 4.1.2 shows a closer look at this storage area environment. The I/O tracks on either side are shared with the adjacent storage areas (except on the chip edges) with the result that most detector and generator regions have four storage areas to support. Connection pads for wire bonding are located on two peripheral edges and in the detector/generator column. Connections to the propagation conductors for the storage areas and the I/O tracks are made at the periphery of the chip. Connections for the gates are made at both the periphery of the chip and in the detector/generator regions. The generators/detectors connections are made entirely in the central column of the chip.

Separate operation of the I/O tracks and the storage areas are intrinsic to the design. A ground return conductor is shared by the two propagation conductors to cancel edge fields. This allows use of the full width of the propagation conductors, the placement of propagation elements such as the I/O tracks and storage areas edge to edge, and the placement of all connection pads at one end of the individual propagation region.

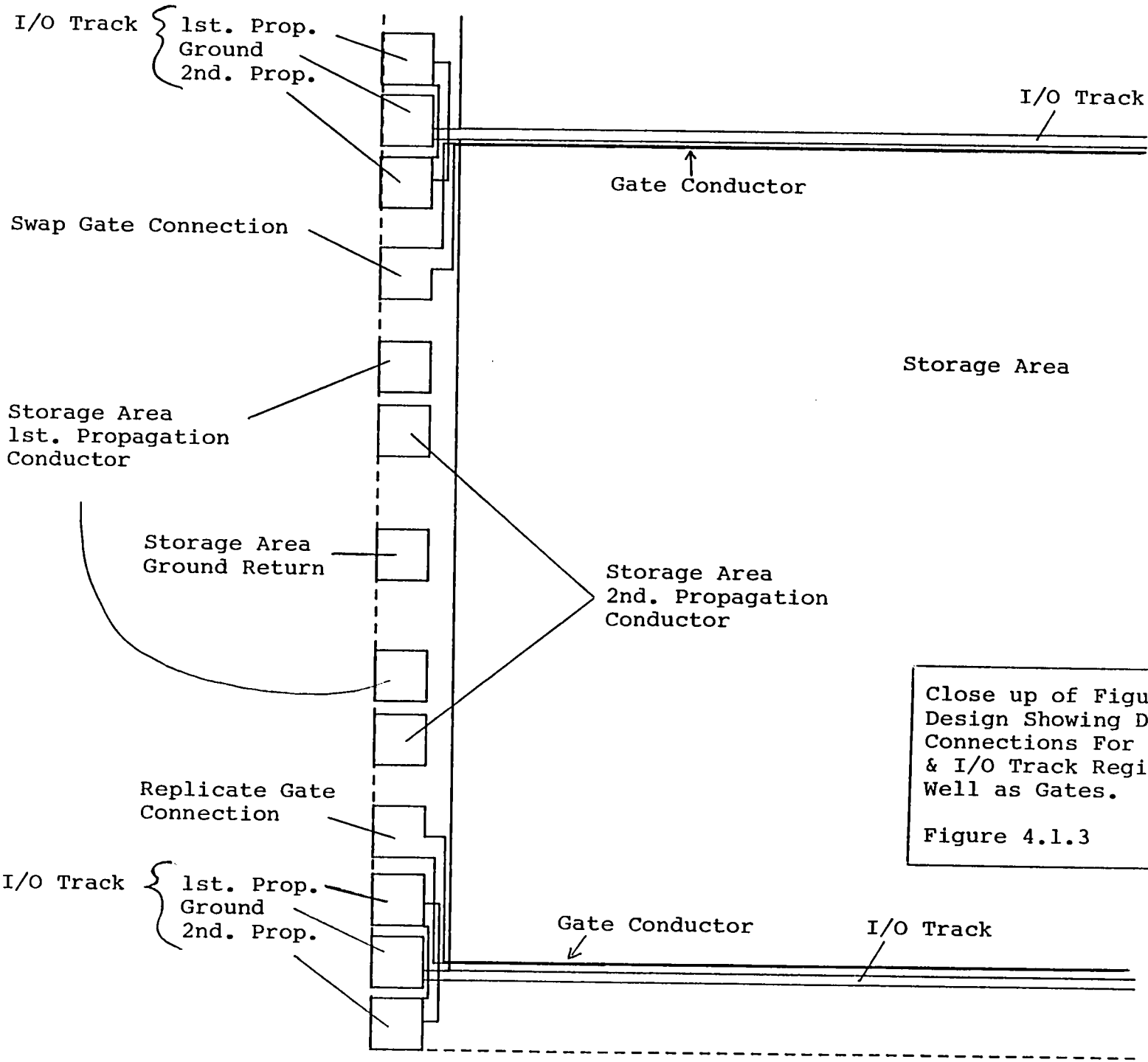
Figure 4.1.3 shows a close up of the die edge of a storage area. As a result of the ground return conductor, there are normally three connections needed for each propagation region (storage areas and I/O tracks). These are indicated for the two I/O tracks which sandwich the storage area. Next to the I/O track pads are the die-periphery connections for the swap and replicate gate conductors. The remaining five pads are connections for the storage area itself. Two pads are used for each propagation layer to more quickly obtain a uniform current density in the conductors. The ground return conductor uses the remaining center pad.

Figure 4.1.4 shows the circuitry in a generator area. Connections are provided for two generators, each of which supports the two storage areas on its side. Moving outwards, the next pads connect to what are at this stage generic data coding conductors. The pattern shown in this figure could generate the in-plane fields needed to switch the bubble state in (110) wall state date coding. Although both (110) data coding conductors (one near each generator loop) would be powered together, only one generator and I/O track would be operating at a time. If independent (simultaneous) operation of a storage area on each side of a generator region was desired, an additional bonding pad could be added. For single/double bubble data coding,two levels of generator current



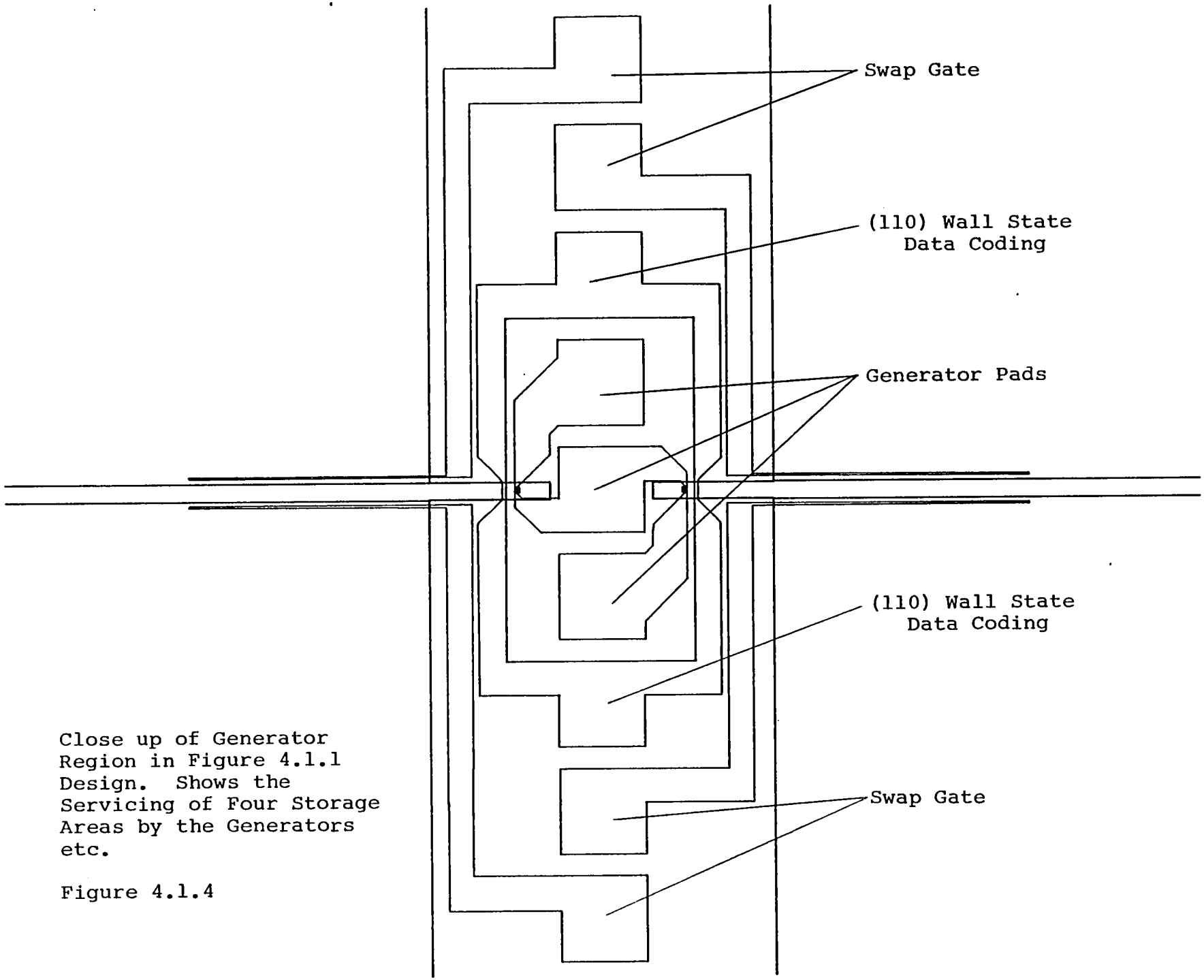

Closer View of Figure 4.1.1 Design Showing Environment
Around Individual Storage Areas.

Figure 4.1.2




Close up of Figure 4.1.1 Design Showing Die Edge Connections For Storage & I/O Track Regions as Well as Gates.

Figure 4.1.3




Close up of Generator Region in Figure 4.1.1 Design. Shows the Servicing of Four Storage Areas by the Generators etc.

Figure 4.1.4

would be used and the additional data coding connections would not be required. The remaining four pads provide connections to the inner end of the four swap gate conductors used for the surrounding storage areas.

Figure 4.1.5 shows a close up of the generators, I/O track positions, data coding conductors, and the gate conductor connections. As shown, the generators are simple hairpin conductors with three connections being used to allow separate control of the two generators.

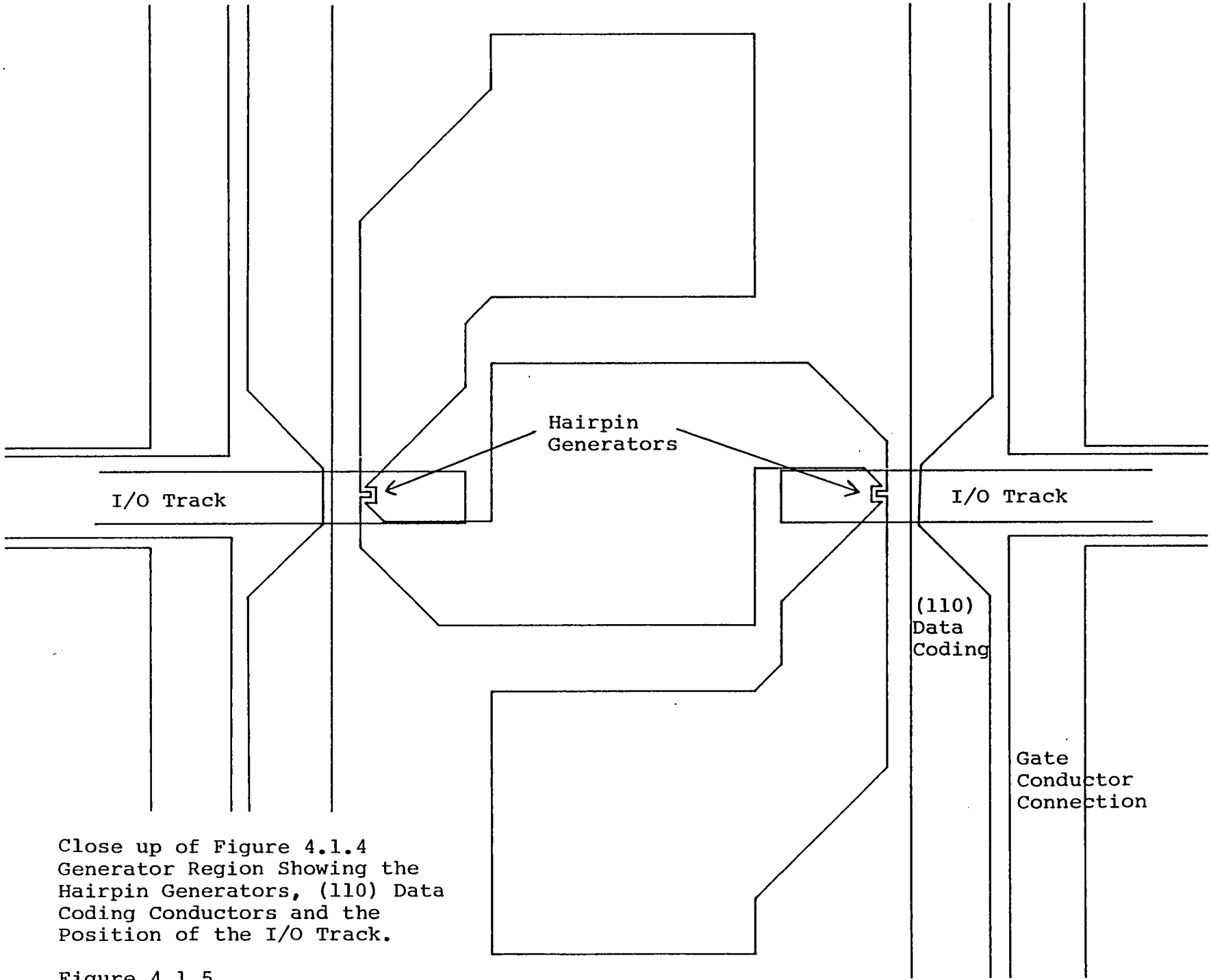
Figure 4.1.6 shows the circuitry in a detector region. Connections are similar to those in the generator regions. In this design, non-stripping detectors are used as shown with two detectors present in each detector region. This allows one detector to be active at a given time and the other to be used as a dummy for noise rejection. Moving outwards, the next pads connect to what are at this stage generic data decoding conductors or discriminators. For the (110) wall state data coding, a conductor similar to that used in data coding will be used for data decoding. An in-plane field is generated which selectively collapses the bubbles according to state. For the single/double bubble coding, a normal field will be generated using a hairpin loop to selectively collapse bubbles. In either case, a discriminator is required before the detector and generic connections are provided in this design.

Figure 4.1.7 shows the generator circuitry and Figure 4.1.8 shows the detector circuitry as modified for the positions at the die edges (see Figure 4.1.1).

18 Storage Region Device-High Pad Count Version: Discussion.

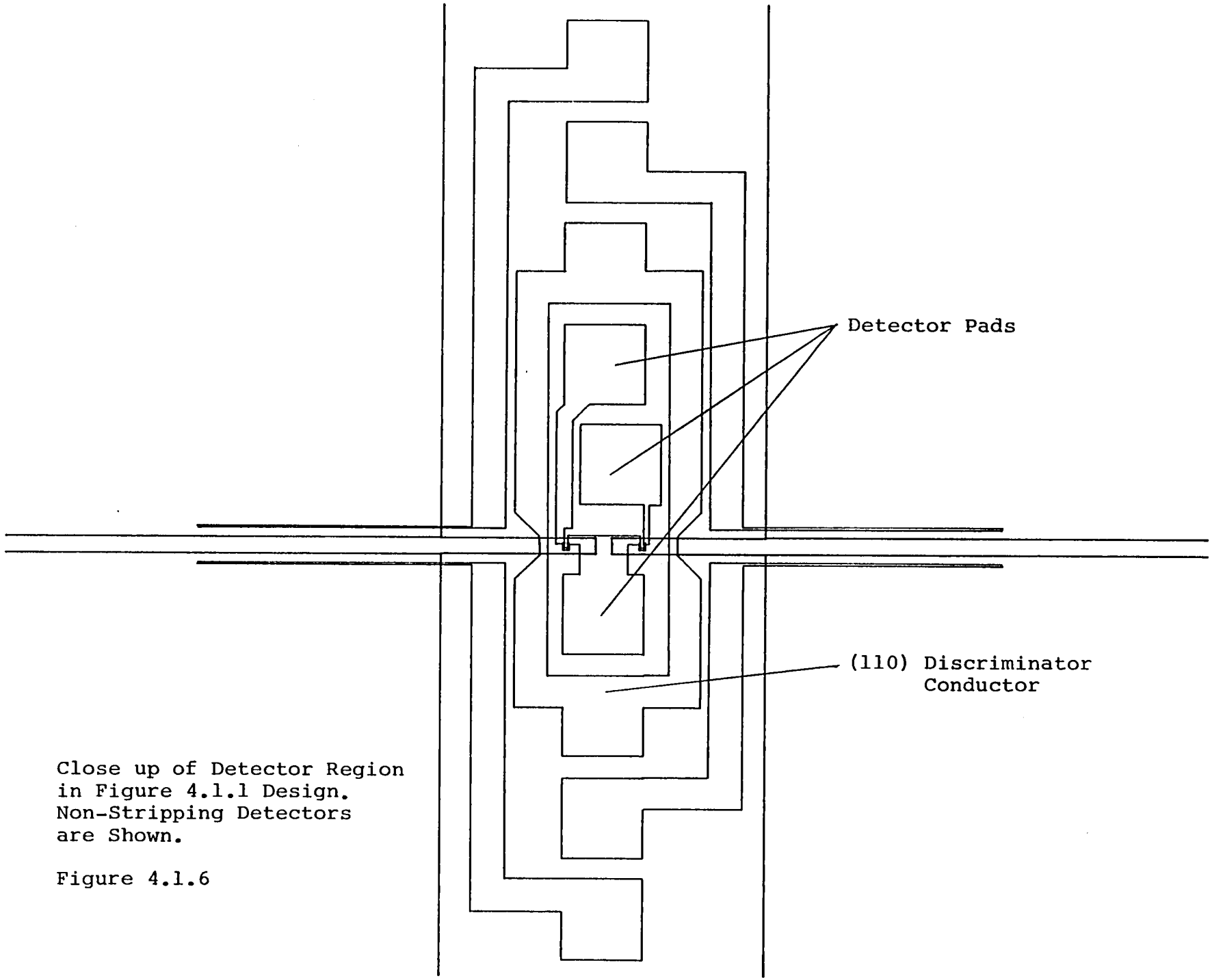
As presented, this 18 storage area design has several weaknesses which will be discussed next. They include data block size, non-uniform current densities at the connection ends of the storage area propagation and ground return conductors, and number, location, and density of the bonding pads.

Possibly least serious is the data block size which results from using as much die area as possible for storage and having a die of 1.5x1.5 cenimeter square. To obtain 640,000 bubbles per storage area with each area having dimensions of 1618x 7150 microns gives 841 storage loops of 760 bubbles (639160 bubbles). With two bubbles being read or written to each loop to fill or empty the I/O track, this gives a block size of 1682 bubbles. To achieve a reasonable power of 2 block size however is easy if the die aspect ratio is changed slightly. If the die is changed from 1.5x1.5 centimeter to 1.38x1.62, the block size becomes 1536 bubbles or 3x512. What data block size is best depends on the future applications of this technology, however, this general approach combined with the fact that the die doesn't have to present a roughly



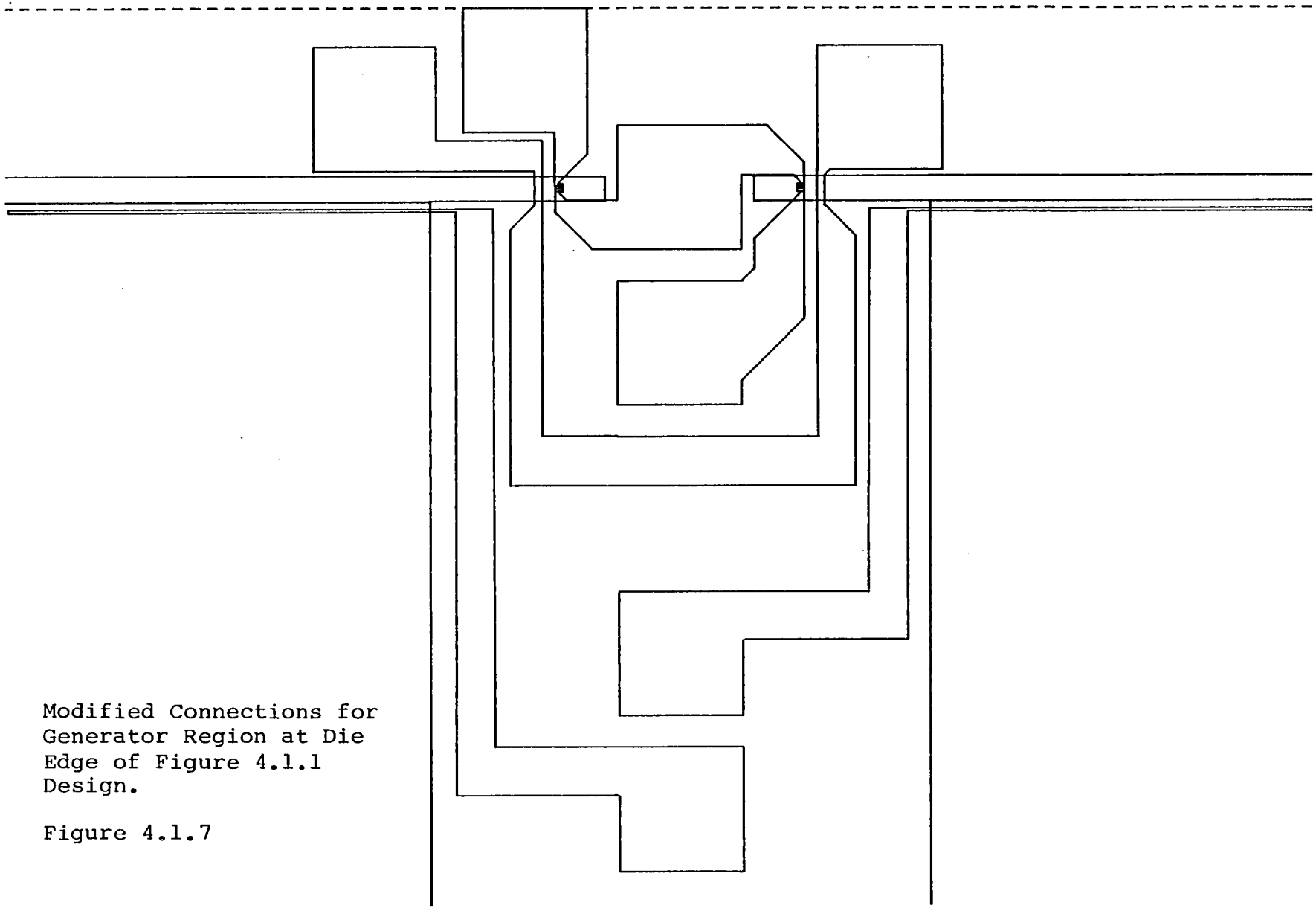

Close up of Figure 4.1.4 Generator Region Showing the Hairpin Generators, (110) Data Coding Conductors and the Position of the I/O Track.

Figure 4.1.5



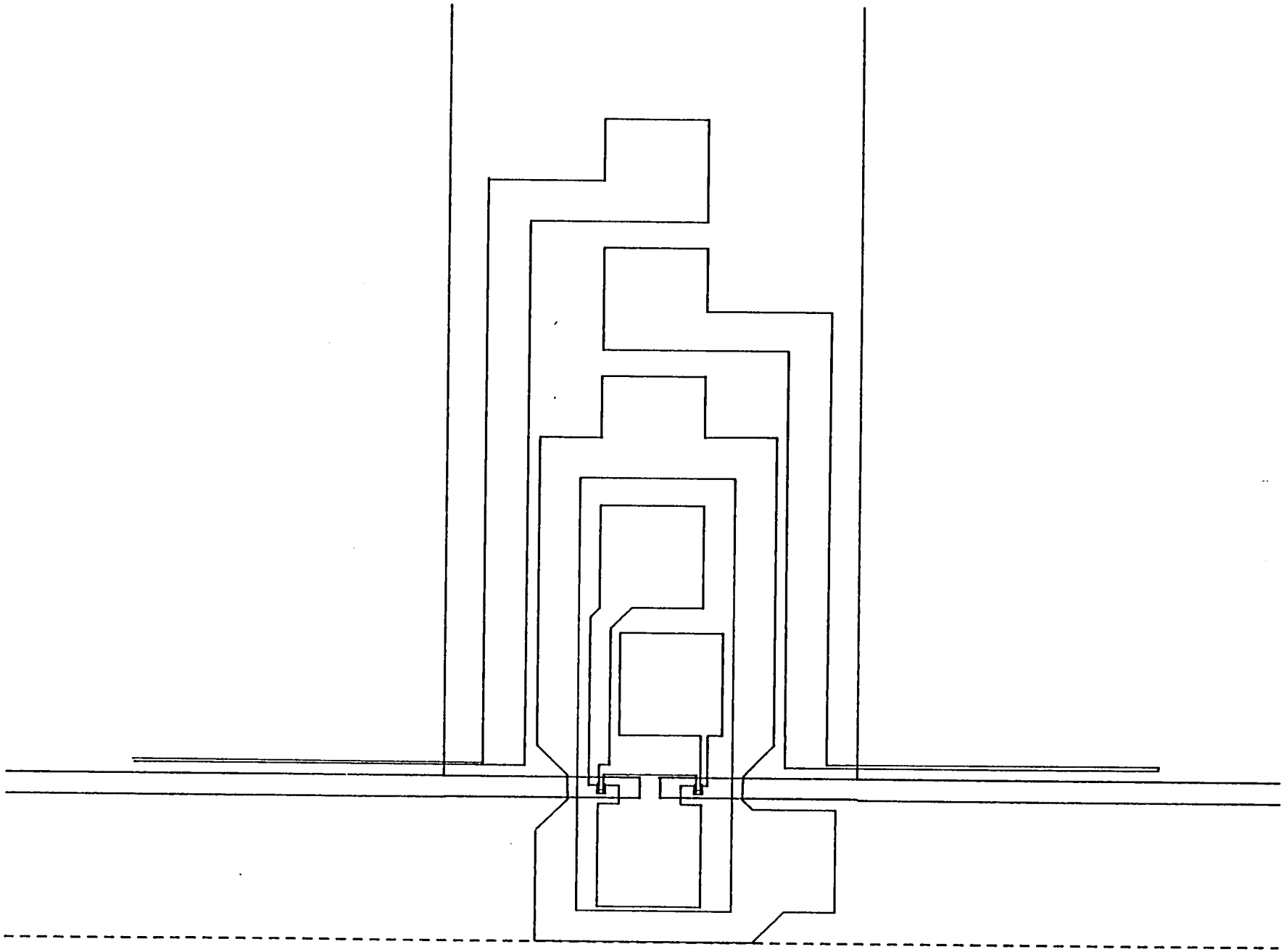

Close up of Detector Region in Figure 4.1.1 Design. Non-Stripping Detectors are Shown.

Figure 4.1.6



Modified Connections for Generator Region at Die Edge of Figure 4.1.1 Design.

Figure 4.1.7



Modified Connections for Detector Region at Die Edge of Figure 4.1.1 Design

Figure 4.1.8

square aspect ratio for in-plane field coils allows for flexibility in achieving a desired block size.

The non-uniform current density at the connection end of the storage area's propagation and ground return conductors is not easily eliminated without sacrificing some of the area efficiency of the chip. By using a few hundred microns of the storage area's length, slots for quickly and accurately spreading out the current from the bonding connection can be fabricated. A 300 micron wide region to fan out the current reduces the storage areas from 92.5% to 92.0% of the chip. This space can also be used to make ground connections with the thick return layer deposition as will be shown in the lower pad count version.

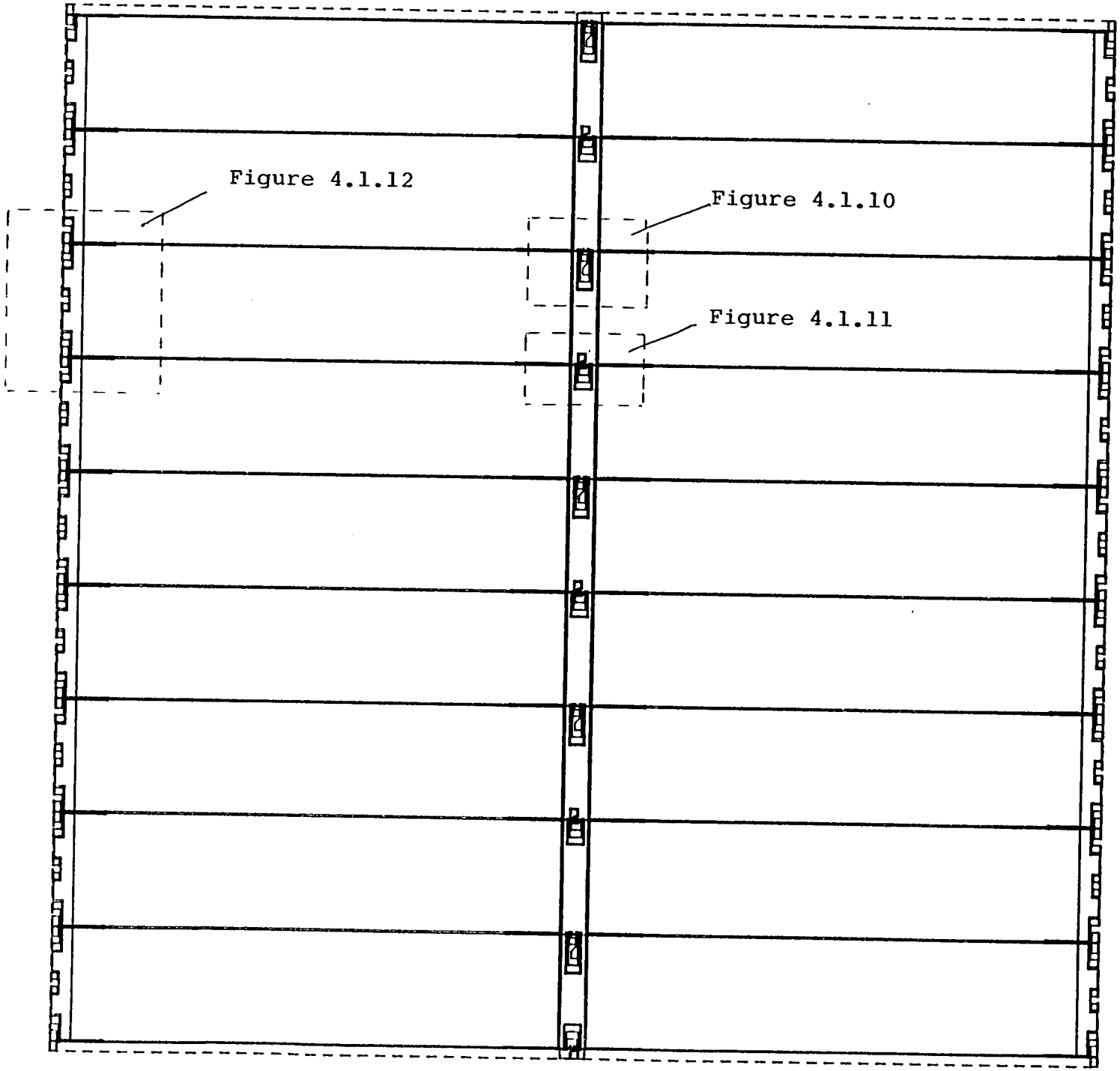
The number of bonding pads and their location is a serious problem in the design as presented in Figure 4.1.1 but can be significantly improved without changing the basic design as will be shown in the lower pad count version covered next.

18 Storage Region Device-Lower Pad Count Version: Physical Description

This device design takes the previous design and basically makes the improvements needed in current uniformity in the storage areas and in bonding-pad count, density, and placement.

The bonding pad count for the first version of this design is 272 with a package pin count of 236 assuming the double pads for each storage areas propagation layers are connected to one package pin. While packages are available to handle this number of connections, it is not desirable from cost, bonding yield, and circuit board complexity points of view to use them. An added complication is that 86 of these 272 pads are not at the edge of the die.

The pad count and package pin count can be reduced considerably by changing the design as shown in Figure 4.1.9. Major reductions are obtained using a common or ground connection for all of the inner gate conductor connections, the central pad for the generators, the central pad for the detectors, one end of the data coding/discrimination conductors, the outer ends of the I/O track return conductors, and the outer ends of the storage areas return conductors. This results in a bonding pad count of 145 if 3 ground pads are provided for left, center, and right ground conductors. This gives a package pin count of 143 assuming the ground pads go to a common pin. Multiplexing schemes such as discussed in Section 2.2 can significantly further reduce the package pin count.




18 Storage Region Design - Lower Pad Count Version. Overall Device is Shown as Well as Areas of 4.1.10 - 4.1.12 Figures

Figure 4.1.9

The next paragraphs will look at this 143 pad version in more detail.

Figure 4.1.10 shows a close up of the detector region. This can be compared to Figure 4.1.6. The main area of the central column is the ground connection conductor. The ends of the replicate gate conductors, one end of the data discriminators, and one end of the detectors are all connected to this ground conductor.

Figure 4.1.11 shows a close up of the generator region. This can be compared to Figure 4.1.4. The ground conductor occupies the main area of the central column again, and similar to the detector region, all elements are appropriately connected to it.

The overall result of the central column ground conductor is to eliminate 55 of the 86 pads in the center column and their package pins.

The common connection approach at the edge of the die for the ground return conductors of the storage areas and I/O tracks is shown in Figure 4.1.12. The area taken from the storage areas for the connection conductor is used in the propagation conductors for obtaining a uniform current density via slots (not shown).

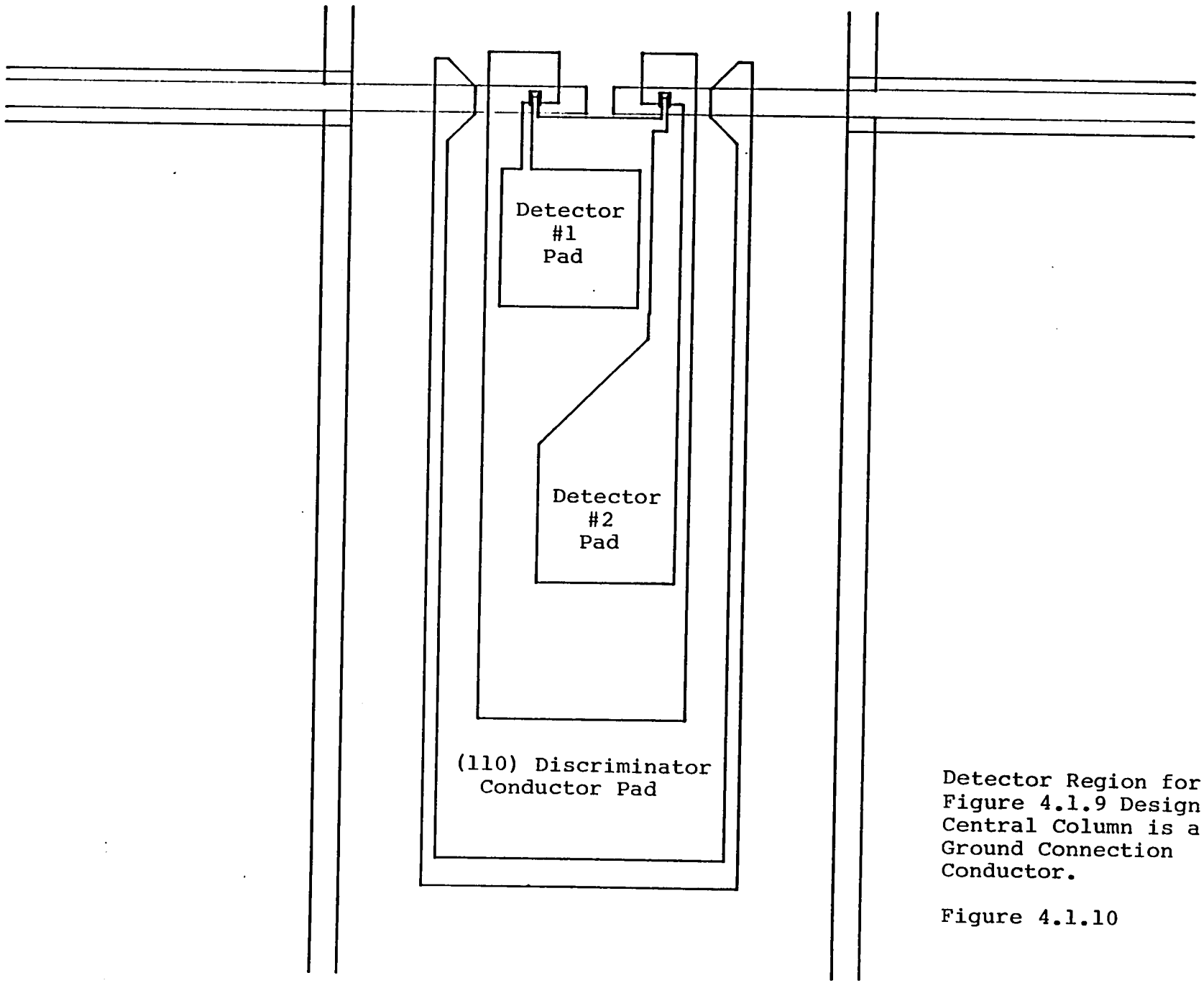
18 Storage Region Device-Lower Pad Count Version: Discussion.

This design makes the general architectural layout of the 18 storage area device much more practical and does it while meeting all of the NASA goals. The 143 pin package count is solidly in the active area of large pin-out package development [ 9 ] but still above the currently practical 124 pin level. At the pace packaging is developing for VLSI circuits with projected needs >300 pins, a 143 pin package may be common place if still not desirable by the time this self-structured approach is fully developed.

A difficulty with multiplexing to reduce the package pin count for this design is that there are a lot of points on opposite edges of the die which must be connected together and no left over die real-estate to make these connections with the conductor layers used. This means that a special package, or complicated wire bonding, or another conductor layer for patterning connections are required for a significantly lower package pin count with this general chip architecture.

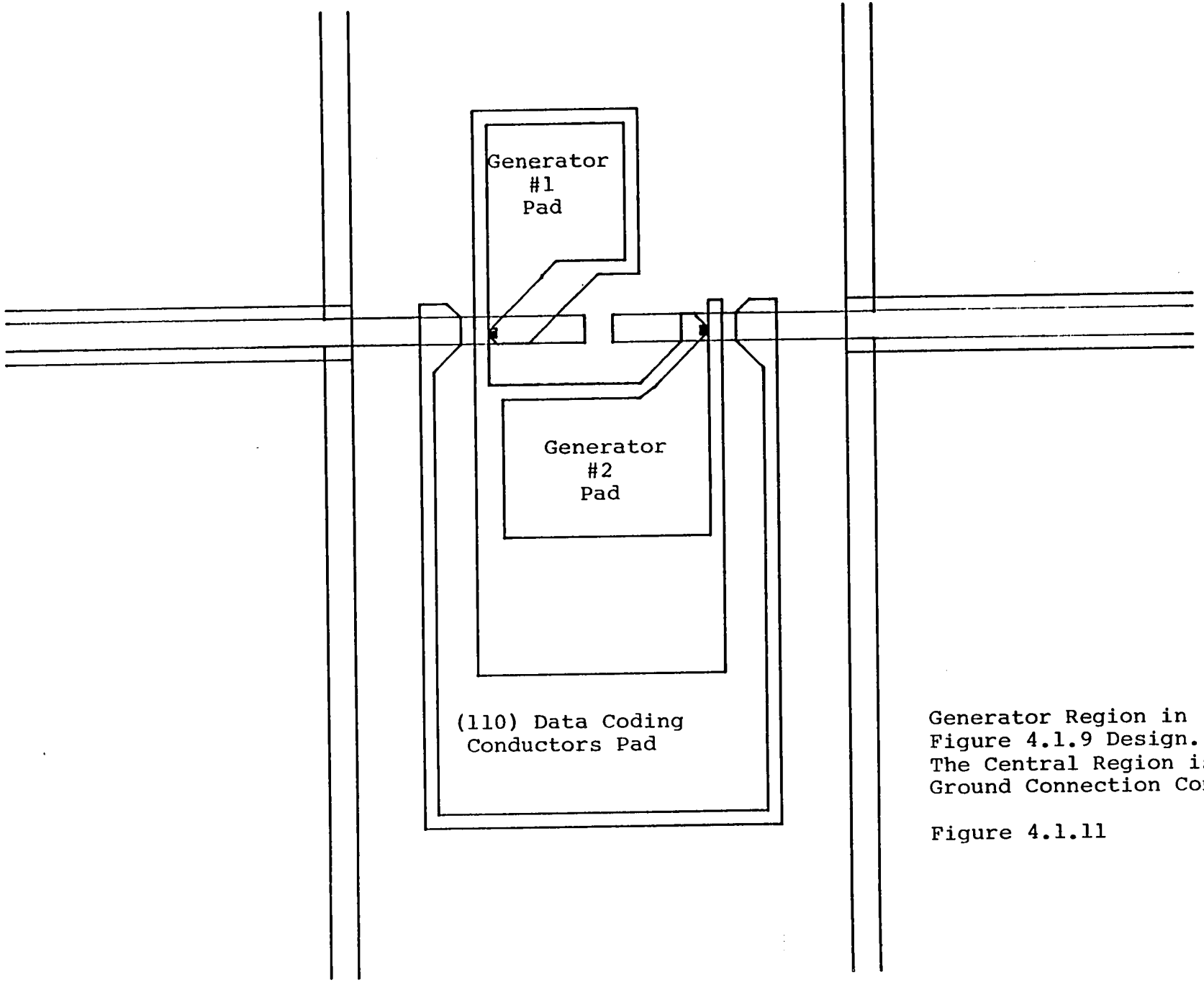
8 Storage Region Device-High Pad Count Version: Physical Description.

The two largest obstacles to a reasonable package pin count and bonding pad count, density, and location, without multiplexing, is the 16 active storage areas and the 2



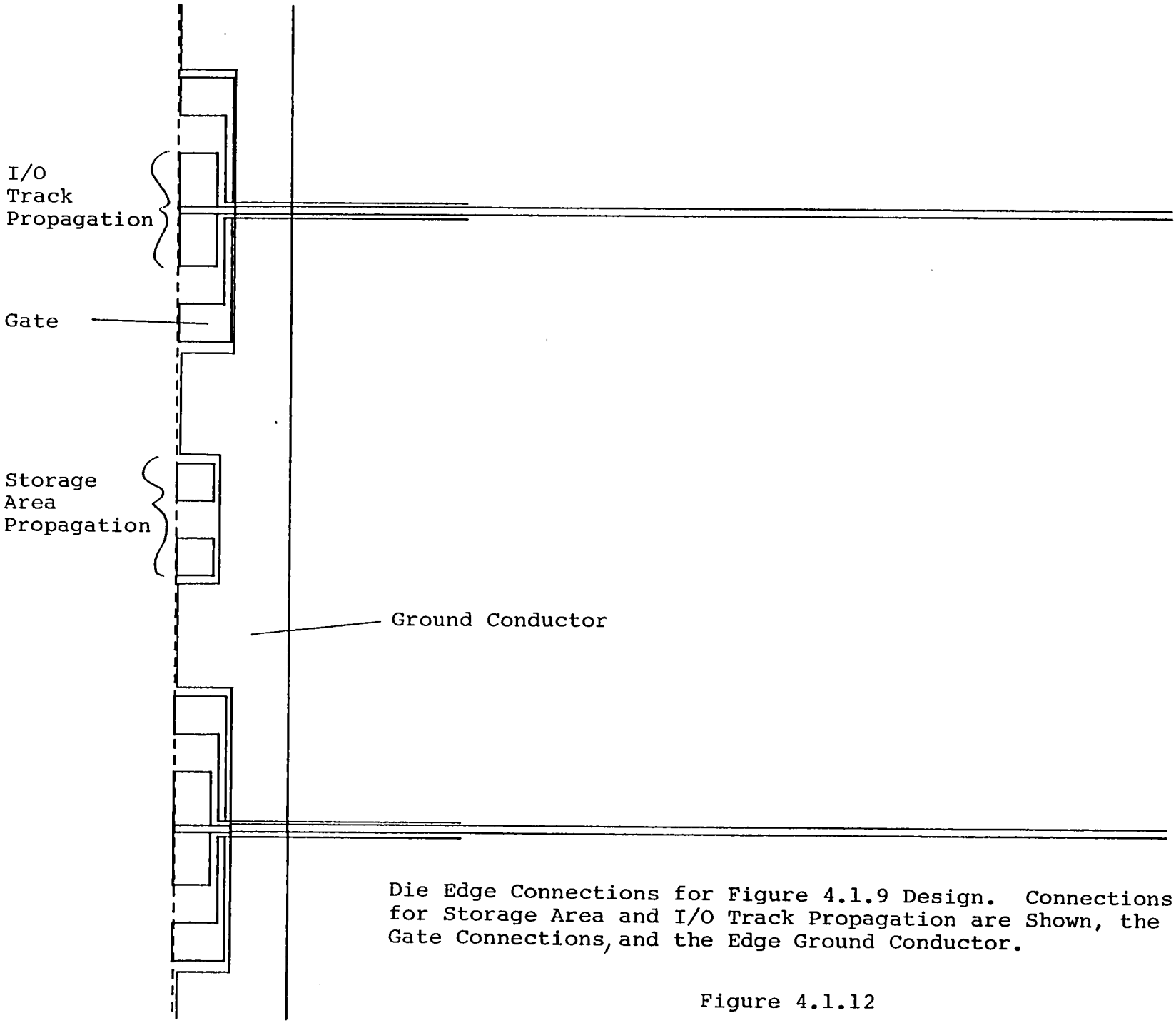

Detector Region for Figure 4.1.9 Design. Central Column is a Ground Connection Conductor.

Figure 4.1.10




Generator Region in
Figure 4.1.9 Design.
The Central Region is a
Ground Connection Conductor.

Figure 4.1.11




Die Edge Connections for Figure 4.1.9 Design. Connections for Storage Area and I/O Track Propagation are Shown, the Gate Connections, and the Edge Ground Conductor.

Figure 4.1.12

redundant storage area approach. Given the demonstrated defect tolerance of the self-structured approach, it seems reasonable to consider a device in which the design assumes that good fabrication yields can be obtained without the redundant areas. In addition, a device with fewer storage areas is useful to consider for comparative purposes. A sufficiently large enough number of storage areas for power dissipation purposes and yet more practical to build and drive than 18 is an 8 storage region device.

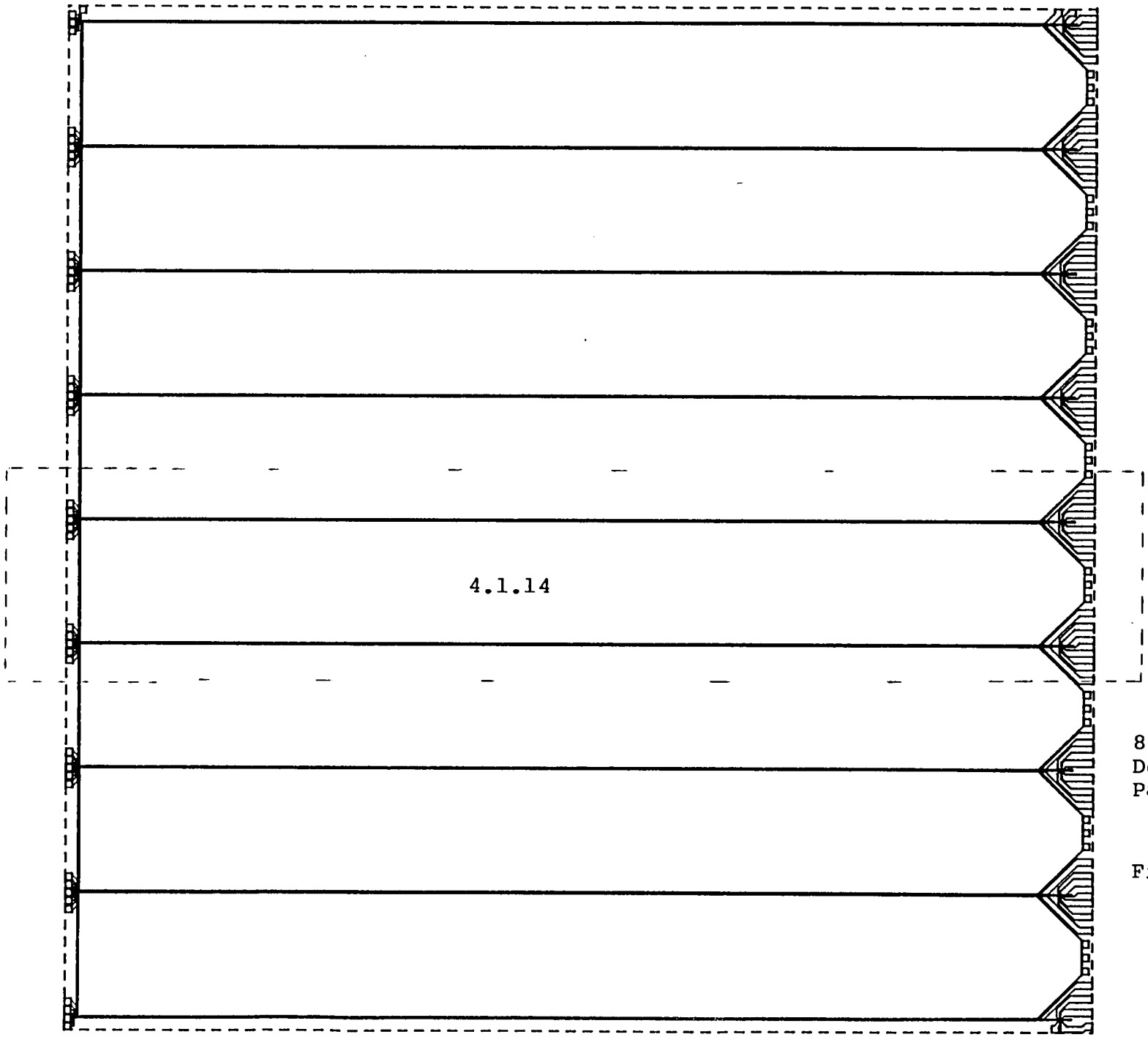
Figure 4.1.13 shows an overview of a device with 8 storage areas, none of which are redundant. As shown, with no common ground or multiplexing approach, all bonding pads are at the die periphery and have sufficient space for convenient bonding (0.004" pads on 0.008" centers). The pad count is 120 which is to be compared with the 272 pads in the equivalently inefficient 18 storage region version.

Figure 4.1.14 shows a close up look at the edges of the device with the middle regions of the storage and I/O track areas omitted. On the one edge of the die, the pads for driving the storage area propagation conductors, generators and detectors, data coding and discrimination conductors, and swap and replicate gate conductors are located. Notice also the tapered ends of the storage area which is used, with slots in the conductors (not shown) to achieve a uniform current density. At the opposite edge of the die are the pads for the I/O track and the gate conductors.

8 Storage Region Device-Lower Pad Count Version: Physical Description

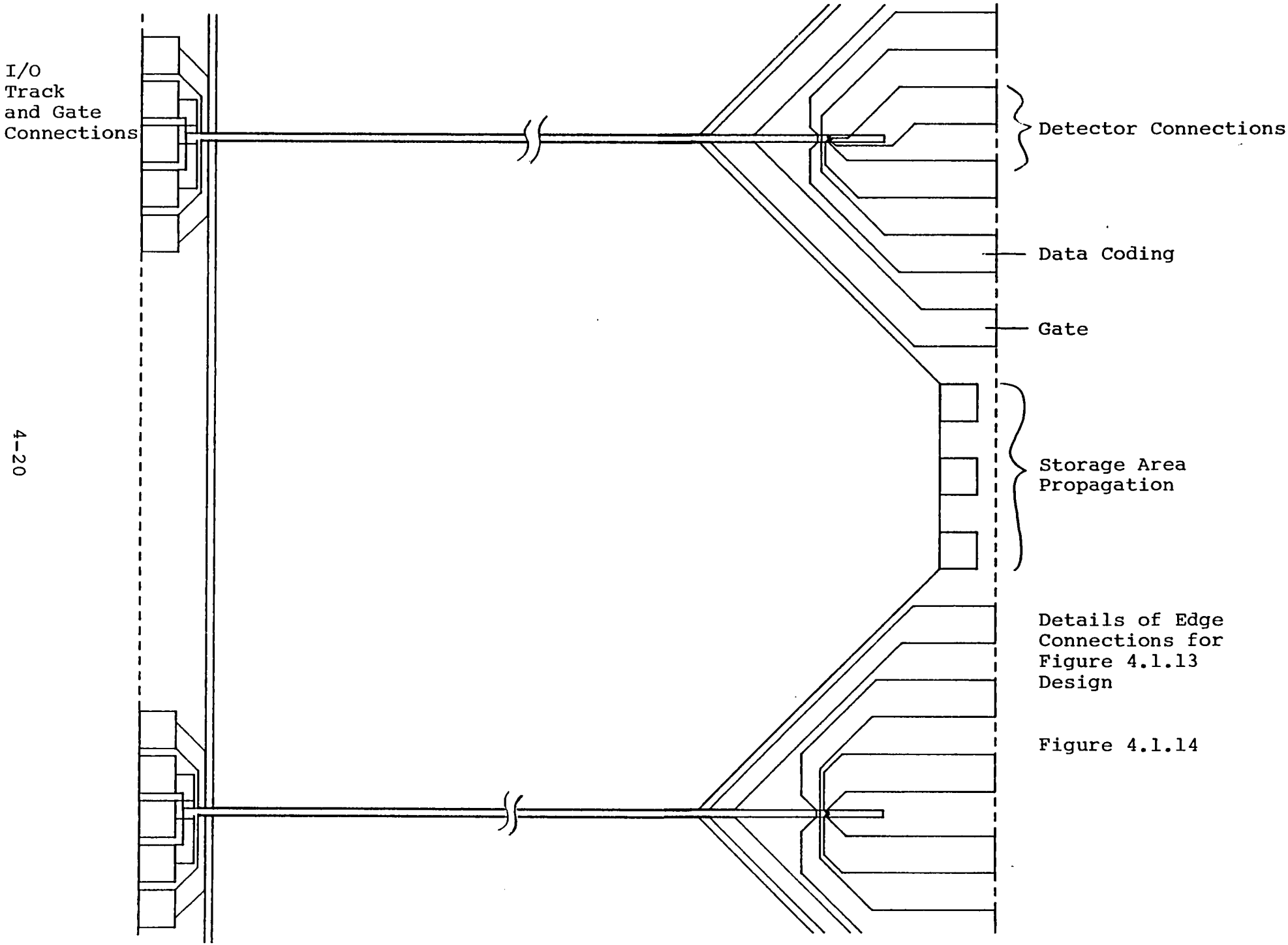
Figure 4.1.15 shows the chip with a common grounding approach taken. The total pad count is reduced to 70 assuming a separate pad on the two 'ground' conductors. The package pin count is reduced to 69 assuming a single ground pin. If single/double bubble data coding is used in which the data coding conductors are not needed, the pad count is reduced to 65 and the pin count to 64. This is getting into reasonable numbers, especially since no pin multiplexing is used.

Figure 4.1.16 shows a close up look at the edges of the device, again with the middle regions of the storage and I/O track areas omitted. The ground conductor on the edge with the generators and detectors is visible as a large triangular region and rectangular sections which skirt around the bonding pads along that edge of the chip and also across the tapered end of the storage areas. The ground conductor at the opposite edge of the chip basically



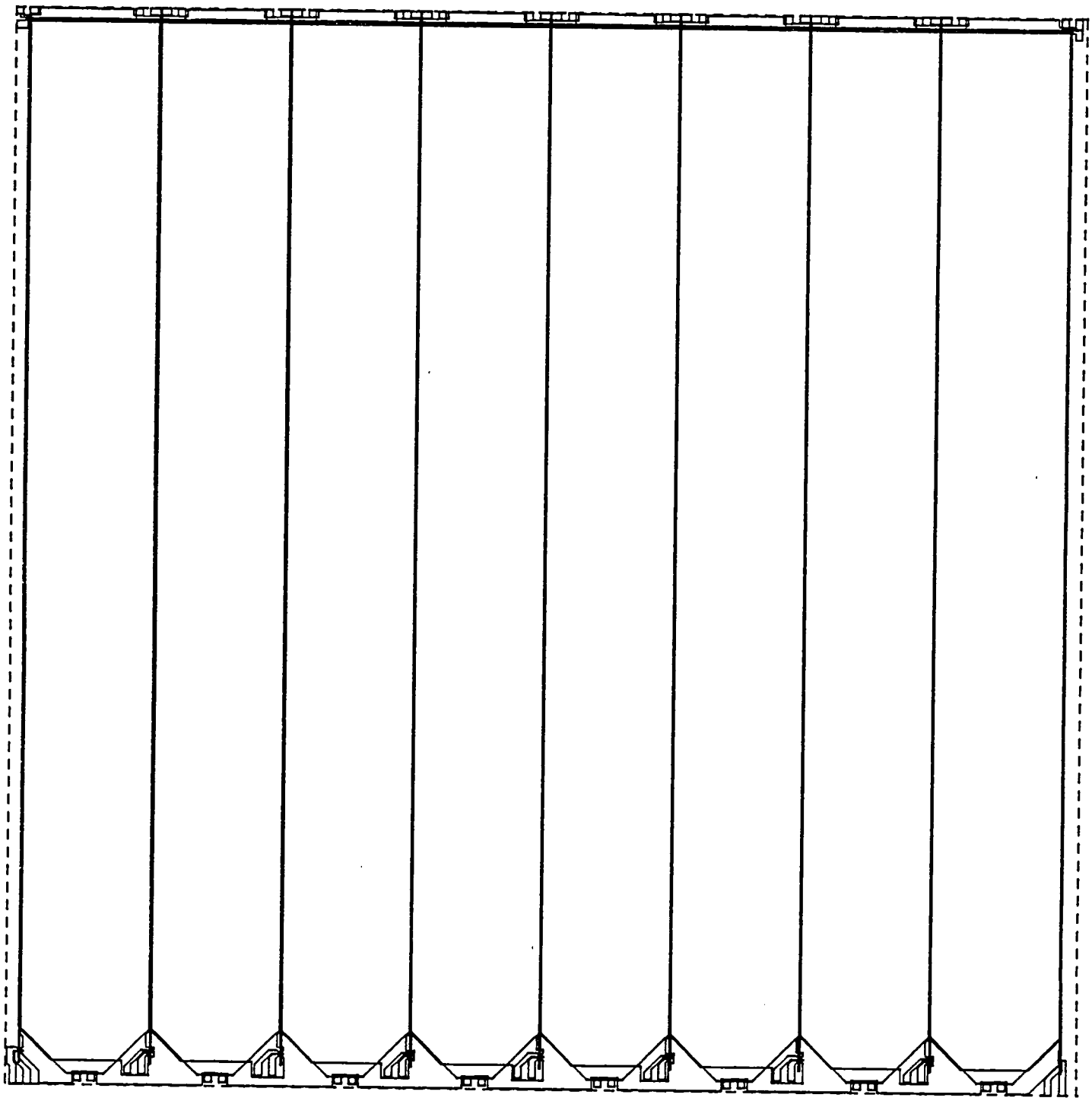

8 Storage Region
Device - High
Pad Count Version.

Figure 4.1.13



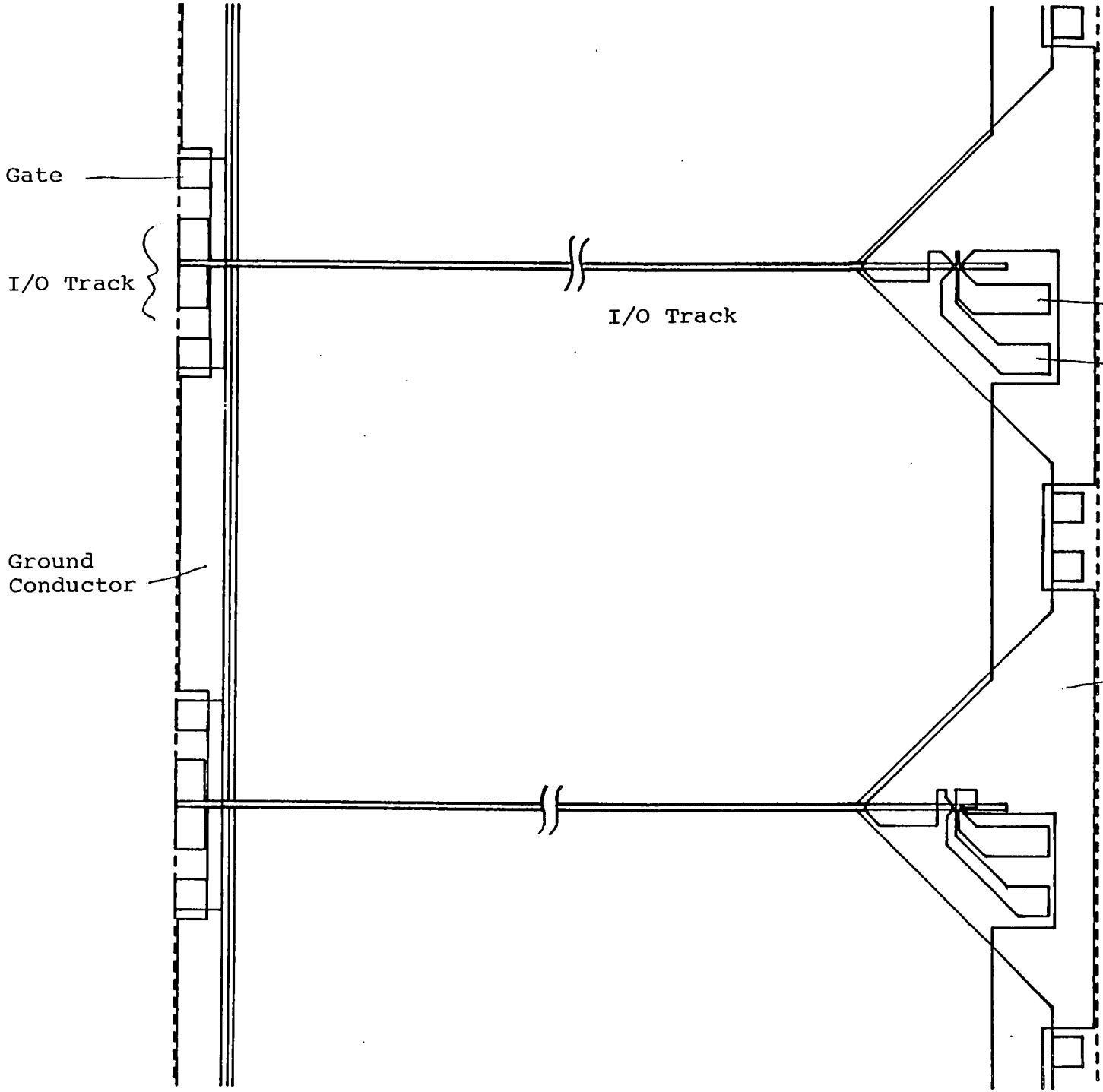

Details of Edge Connections for Figure 4.1.13 Design

Figure 4.1.14



8 Storage Region Device - Lower Pad Count Version

Figure 4.1.15




Close up of Edge Connections for Figure 4.1.15 Design

Figure 4.1.16

fills the space between the ends of the storage areas and the edge of the die. It jogs around the bonding pads on this edge of the chip. On both edges, the thick deposition used for the return conductors in the storage and I/O track areas can be used for the ground conductor to give minimum resistance connections.

8 Storage Region Device-Lower Pad Count Version: Discussion

This device's architecture (Figure 4.1.15) and general connection approach appears to be the best structure from a power consumption, bonding, pin count, and device control overall compromise. By varying the aspect ratio of the chip, read and write block sizes of from 2K - 4K bits are possible. All bonding pad connections are at the edge of the die with 0.004" pads on minimum 0.008" centers. The ground connection conductors at both ends of the chip can be formed from the thick conductor deposition used in the storage and I/O return conductor layer. Finally, there is room in the detector regions to substitute a stripping detector (and additional connection pads if required) in place of the non-stripping detectors shown.

Overall, this design provides a viable goal for guiding the ongoing Sperry funded effort which will continue after this contract.

Access Times for the 8 and 18 Area Designs

Data access times are functions of design geometry and data rates. The results given here reflect 1.5 MHz and (and expected) 15. MHz data rates as typical of the (111) garnet and (110) garnet materials, respectively. The average access time for the first bit out in a 3364 bit data block with the 18 storage area design is 0.25 ms at 1.5 MHz and 0.025 ms at 15 MHz. The 8 storage area design (with 1566 storage loops and 804 bubbles per loop) has an average access time to 0.27 ms to begin readout of a 3132 bit data block at a 1.5 MHz data rate. The 15. MHz data rate reduces this average access time to 0.027 ms.

## 4.2 Power and Thermal Requirements

This modeling assumes 18 storage areas of 831 loops of 752 bubbles in the device architecture shown in Figure 4.1.1.

### 4.2.1 Power dissipation as a Recorder (Read or Write Mode)

The first set of calculations in this section are for power dissipation of the 10 Mbit chip operating in a read or write recorder mode. In this mode data is written or read in a sequential fashion with minimal bubble motion and hence minimal power consumption at the 1.5 MHz data rate.

One storage area and the adjacent I/O track will cycle twice to move two bubbles from each storage loop into the I/O track (or vice versa for writing). Then the storage areas wait for 1662 cycles while the I/O track empties (or fills). This process then repeats as necessary. The duty cycle for the storage area is $d_s$ where

$$d_s = 2/1664 = 0.0012.$$

The aluminum drive layer thicknesses will be assumed to be 250 nm and 350 nm for the first and second layers respectively. The electrical resistance for a conductor layer is given by

$$R = \frac{\rho L}{tw}$$

where $\rho$ = resistivity $(2.5) \times 10^{-8}$ ohm-m for aluminum)

$L$ = length

$t$ = thickness

and $w$ = width of the conductor.

For the lower (or first) layer

$$R_1' = \frac{(2.5 \times 10^{-8}\ \Omega\text{-m}) \times (0.007150\text{m})}{(0.25 \times 10^{-6}\text{m}) \times (0.001618\text{m})}$$

$$= 0.442\ \Omega$$

For the upper drive layer

$$R_2' = R_1' \times \frac{250.\text{nm}}{350.\text{nm}}$$

$$= 0.316\ \Omega$$

The resistance $R_1'$ and $R_2'$ must now be corrected for the presence of apertures in each sheet. A variety of approaches can be used to make this correction either making approximations or doing an exact calculation. Two quick calculations are given below which bracket the exact answer after which the largest correction is chose to provide a conservative result.

A first order general approach is to consider a sheet with N apertures with length L and width W as shown in Figure 4.2.1. If the sheet is divided into 2N + 1 segments by extended vertical lines along the edges of the apertures, the total resistance is given by

$$R = \sum_i \frac{\rho L_i}{t w_i}$$

where $L_i$ is the (horizontal) length of each segment,

$w_i$ is the net (vertical) width of each segment,

$t$ is the conductor thickness, and

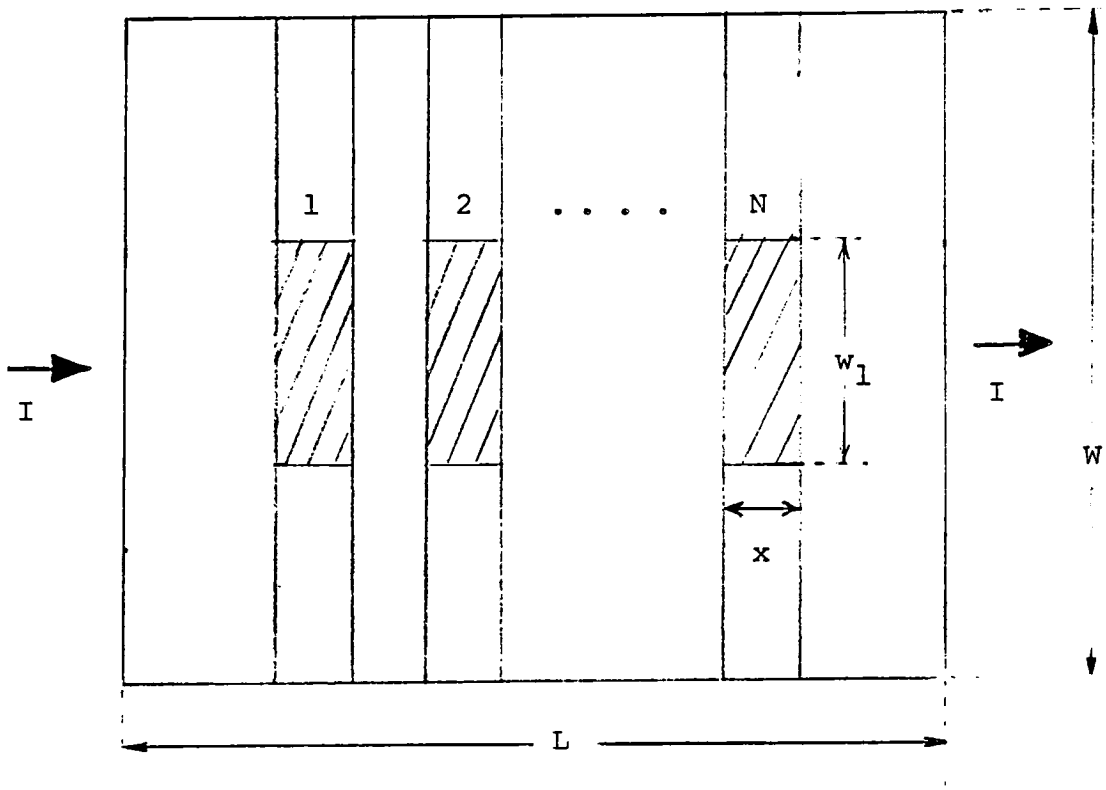
$\rho$ is the resistivity.

If there are N apertures (or vertical rows of apertures as in the real device), each of length x, then

$$R = \frac{\rho}{t} \sum_i \frac{L_i}{w_i}$$

$$= \frac{\rho}{t} \left[ \frac{L - Nx}{w} + \frac{Nx}{W - w_1} \right]$$

$$= \frac{\rho}{t} \frac{L}{w} \left[ 1 - \frac{Nx}{L} + \frac{Nx}{L\left(1 - \frac{w_1}{w}\right)} \right]$$




Geometry used for correction of resistance due to the presence of apertures.

Figure 4.2.1

For the data storage areas of the 10 Mbit chip designed for this report,

$w_1/W = 1/2$

N = 1662 (831 storage loops each having two sides)

x = 2 microns

L = 7150 microns.

Inserting these numbers into the formula above gives

$$R = \frac{\rho L}{tw} \quad (1.45)$$

or a 45% increase in resistance due to the presence of the apertures.

A better correction would adjust for the fact that current flow will not be uniform near the apertures. Rather than doing this exact calculation it is noted that if the apertures were long enough that they touched, the resistance increase would be a factor of two since $w_1/W = 1/2$. Thus the real correction factor must be between 1.45 and 2.0. For the purposes of this report the factor of two increase in resistance due to the presence of the apertures will be used for both the storage areas and the I/O track (which have the same nominal aperture geometry). Thus $R_1 = 2R_1' = 0.886\Omega$ and $R_2 = 2R_2' = 0.632\Omega$.

Storage Loop

A 1.5 MHz propagation frequency ( data transfer rate) with pulses having 33% overlap at each end requires 250 ns pulses with a duty cycle, $d_\lambda$, during access, equal to 0.75 for each conductor. Thus the average power dissipated in the recorder mode will be, with conductors of W width in both layers:

$$(P_{rec}) = d_s \times T \times d_\lambda \left[(J_1^2 R_1 + J_2^2 R_2) W^2\right].$$

Recall that $d_s$ is the fraction of time the storage area is being accessed and J is the linear current density (usually expressed in mA/μm). T is a unitless factor to account for the power dissipation in a third level return conductor to return the current to the chip edge.

Note that a thin return sheet will tend to cancel the edge effect normal fields of the current sheet. This is desirable to maintain a uniform bias field over the chip. Another advantage is the elimination of midchip bonding requirements for the drive layers. The disadvantages are the factor of T increase in power dissipation and the increase in the number of deposition layers. In the numerical analysis to follow the following values of T will be used to show the effect of the power dissipated in the return conductor:

T = 1.0 -- equivalent to no return conductor

T = 1.5 -- equivalent to a return conductor with thickness equal to twice the conductor drive layer. Thicker thicknesses would give 1.0 < T < 1.5.

A real device would probably use a T between these values.

If it is assumed that $J_1 = J_2 = J$ and W = 1618 microns, the average power dissipated by one storage area in the recorder mode, $\langle P_{s,rec} \rangle$, is given by

$$\langle P_{s,rec} \rangle = d_s \times T \times d_\lambda \times J^2 \times (1618\mu m)^2 \left[R_1 + R_2\right]$$

$$= 3.6 \times 10^{3} \; TJ^2 \; \mu watt$$

$$= 3.6 \times 10^{-3} \; TJ^2 \; watts$$

with J in units of mA/micron.

I/O Track

It is assumed for the I/O track power dissipation that:

1) the thicknesses of the conductor layers are the same as for the storage area (250 nm and 350 nm),

2) the I/O track has a length of 7150 microns and is 20 microns wide (as per section 4.1), and

3) the track runs with a duty cycle of one.

The resistance for the lower conductor is given by

$$R_3 = 2 \times \frac{(2.5 \times 10^{-8}\Omega\text{-m})\ (0.00715\ \text{m})}{(250 \times 10^{-9}\text{m})\ (20 \times 10^{-6}\text{m})} = 71.6\Omega$$

and for the upper drive conductor,

$$R_4 = R_3 \times \frac{250\text{nm}}{350\text{nm}} = 51.1\Omega$$

where the leading factor of 2 comes from the aperture correction discussed above. The average power dissipated in the I/O track in the recorder mode is

$$\begin{aligned} \langle P_{I/O,\ rec} \rangle &= T\ (0.75)\ J^2\ (20\mu\text{m})^2\ (71.6\Omega + 51.1\Omega) \\ &= 3.7 \times 10^4\ TJ^2\ \mu\text{w} \\ &= 0.037\ TJ^2\ \text{watts with J in mA/micron.} \end{aligned}$$

Swap Gate

The swap gate conductor is essentially a 4 micron wide by 8125 micron long conductor of 500 nm thickness. The resistance is given by

$$R_{SG} = \frac{(2.5 \times 10^{-8}\Omega\text{-m})\ (8125 \times 10^{-6}\text{m})}{(500 \times 10^{-9}\text{m})\ (4 \times 10^{-6}\text{m})}$$

$$= 101\ \text{ohms.}$$

The power dissipation at 100% duty cycle for the swap gates for I = 20 mA

$$P_{SG}\big|_{100\%} = (101\Omega)\ (0.02\text{A})^2$$

$$= 0.04\ \text{watt.}$$

With a duty cycle d = 0.0012 (same as the storage area above), the average power consumption is given by

$$\langle P_{SG} \rangle = (0.0012)\ (0.04w)$$

$$= 0.00005 \text{ watt}$$

Replicate Gate

The block replicate gate conductor is a 2 micron wide by 35000 micron long conductor of 500 nm thickness. Its resistance will be

$$R_{RG} = \frac{(2.5 \times 10^{-8} \Omega\text{-m})\ (35000 \times 10^{-6} \text{m})}{(500 \times 10^{-9} \text{m})\ (2 \times 10^{-6} \text{m})}$$

$$= 875 \text{ ohms.}$$

The power dissipation at 100% operation of the replicate gates is

$$P_{RG}|_{100\%} = R_{RG} I^2 = (875\Omega)\ (20\text{mA})^2$$

$$= 0.35 \text{ watts}$$

With a duty cycle of 0.5 $d_s$, the average power consumption is

$$\langle P_{RG} \rangle = (0.5)\ (0.0012)\ (0.35w)$$

$$= 0.00021 \text{ watts.}$$

Detectors

Power dissipation in the detectors will, of course, depend on the type of detector in use. The non-strip-out detectors which this report describes will dissipate less power than strip-out detectors with their longer permalloy strips. It is assumed that the sensing currents would be similar in the

two types of detectors. As will be shown below the power dissipation problem for detectors is not serious. This report shall choose the strip-out detector as a worst case example.

Assuming that only one detector (of the five on the chip) is operating at any one time, the resistance for an 80 micron long by 2 micron wide by 35 nm thick permalloy element is given by

$$R = \frac{(18 \times 10^{-8}\Omega\text{-m}) \quad (80 \times 10^{-6}\text{m})}{(2 \times 10^{-6}\text{m}) \quad (35.0 \times 10^{-9}\text{m})}$$

$$= 206 \text{ ohms.}$$

For a 4mV detection signal, assuming a conservative 0.5% magneto-resistive $\Delta\rho$, the necessary drive current is

$$I_{DET} = \frac{\text{signal level}}{\Delta\rho \times R_{DET}}$$

$$= \frac{0.004 \text{ v}}{0.005 \times 206\Omega}$$

$$= 0.0039 \text{ A}$$

Power dissipation in the detector is

$$P_{DET} = (I_{DET})^2 R_{DET} = 0.0031 \text{ w.}$$

If a dummy detector is also used in a bridge detector circuit this power will be doubled. It should be noted here that tests with the aperture drive have shown that a dummy detector on the chip may not be necessary for noise cancellation as required in field accessed devices. For the purposes of this report a detector power consumption of 0.0062 watt will be used.

Discriminator

For "single-bubble/double bubble" data coding a normal field needs to be applied while the bubble attempts to strip out 4 . Discrimination is achieved by the selective stripping out due to the two types of bubbles. Specific circuits to do this have not been developed and therefore are not modeled here. The results of the (110) garnet discriminator will be used in the subsequent power dissipation studies.

For (110) garnets with orthorhombic anisotropy and wall state coded data, an in-plane field component of 25 G must be provided in an area on the order of a storage cell for bubble discrimination. Assuming a conductor with dimensions of 4.5 microns wide, 8 microns long, and 500 nm thick the resistance $R_{DIS}$ is given by

$$R_{DIS} = \frac{(2.5 \times 10^{-8}\Omega\text{-m})\ (8 \times 10^{-6}\text{m})}{(4.5 \times 10^{-6}\text{m})\ (500 \times 10^{-9}\text{m})}$$

$$= 0.10\Omega.$$

Since the magnetic field along the surface of a current sheet has a magnitude of 6.3 G per mA/micron, the required current to give a 25 G field will be

$$I = \frac{(25\ G)\quad (4.5\mu m)}{(6.3\ G/mA/\mu m)} = 0.0179\ A.$$

Power dissipation in this discriminator at 100% operation is given by

$$P_{DIS}|_{100\%} = I^2\ R_{DIS}$$

$$= (0.0179A)^2\ (0.10\Omega)$$

$$= 3.2 \times 10^{-5}\ \text{watt.}$$

The average power dissipation is given by

$$\langle P_{DIS} \rangle = (1 - d_s) \times 1/4 \times P_{DIS}|_{100\%}$$

where the 1/4 factor is the duty cycle within one propagation interval. Thus

$$\langle P_{DIS} \rangle = (1 - 0.0012)\ (0.25)\ (3.2 \times 10^{-5} w)$$

$$= 8.0 \times 10^{-6}\ \text{watts.}$$

Generation

Details on generation (or data coding) will have to wait for decisions to be made on data coding requirements. For this report it will be assumed that conventional generation with a hairpin conductor is used and data coding is ignored. The hairpin conductor surrounds a nominal 2 micron area. The resistance will be given by

$$R_G = \frac{(2.5 \times 10^{-8}\Omega\text{-m})\ (13 \times 10^{-6}\text{m})}{(2 \times 10^{-6}\text{m})\ (500 \times 10^{-9}\text{m})}$$

$$= 0.325 \text{ ohms.}$$

The field required is nominally given by $H_k - 4\pi M =$ constant. Thus the current required for the 6 micron generators (in the work done under this contract) should also apply for 2 micron bubbles. The present studies required 120 mA. The continuous power dissipated will be given by

$$P_G|_{100\%} = (0.12A)^2\ (\ 0.325\Omega)$$

$$= 0.0047 \text{ watts.}$$

The average power assuming 200 ns pulses in the 666 ns propagation period is given by

$$\langle P_G \rangle = \frac{200}{666}\ (1 - d_s)\ P_G|_{100\%}$$

$$= 0.3\ (1 - 0.0012)\ 0.0047w$$

$$= 0.0014 \text{ watts.}$$

Summary of Power Dissipation in the Recorder Mode

For the writing mode as a recorder the total power dissipation can be determined by adding up all of the operating segments from above as required for inputting data at 1.5 MHz.

| | | | |
|---|---|---|---|
| Writing: | storage area | $P_S$ | = 3.6 T $J^2$ mW |
| | I/O track | $P_{I/O}$ | = 37 T $J^2$ mW |
| | block swap gate | $P_{SG}$ | = 0.05 mW |
| | generator | $P_G$ | = 1.4 mW |

The sum of these four terms is $P = 40.6\ T\ J^2 + 1.5$ mW. This function is plotted in Figure 4.2.2 (for T values of 1.0 and 1.5) as a function of the current density in the conductor sheet.

The power requirements for the read mode are summarized below:

| | | | |
|---|---|---|---|
| Reading: | storage area | $P_S$ | = 3.6 T $J^2$ mW |
| | I/O track | $P_{I/O}$ | = 37 T $J^2$ mW |
| | block replicate gate | $P_{RG}$ | = 0.21 mW |
| | discriminator | $P_{DIS}$ | = .008 mW |
| | detector | $P_{DET}$ | = 6.2 mW |

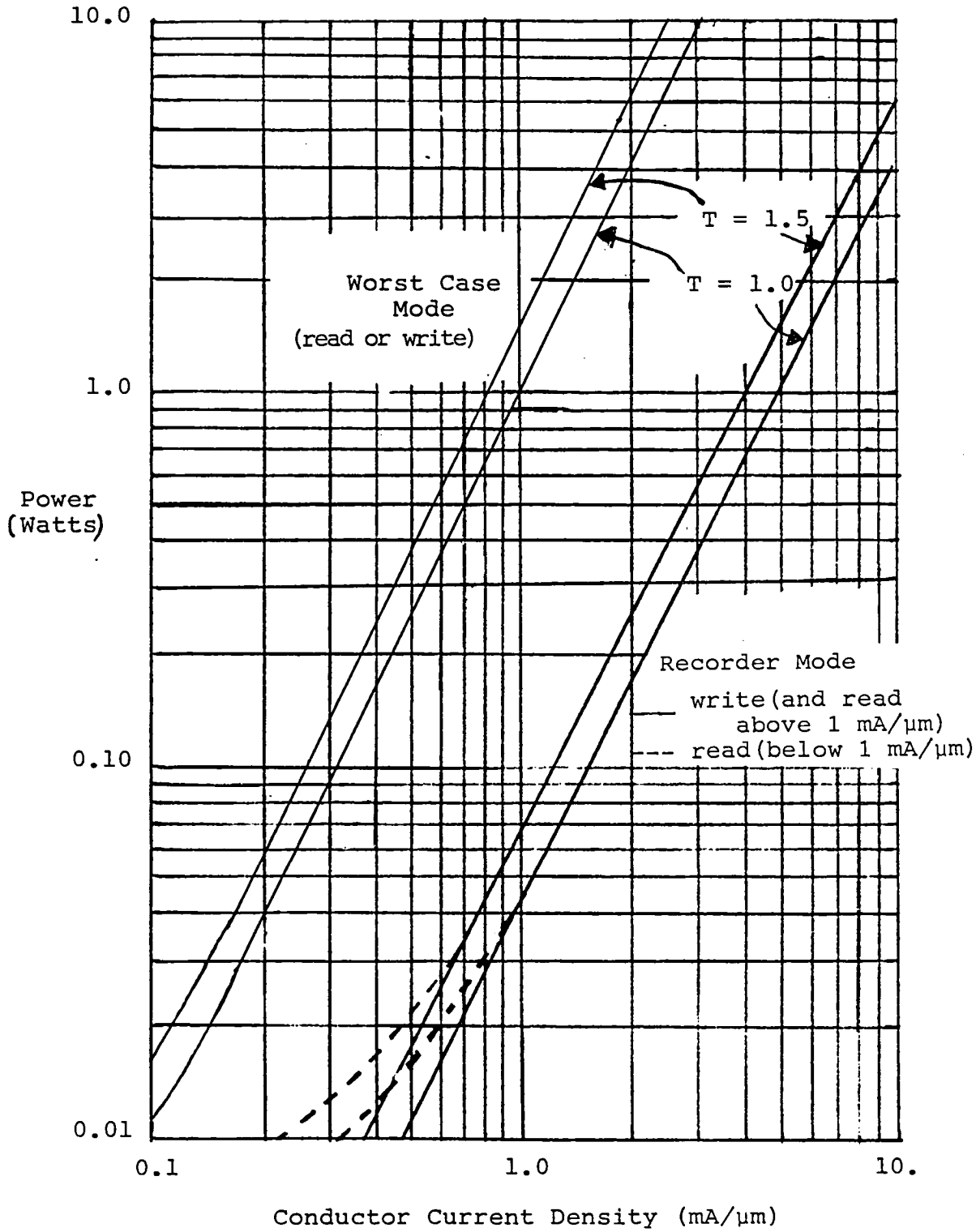
The sum of these terms is given by 40.6 T $J^2$ + 6.4 mW. This result is, for all practical purposes, identical to the result for the write mode for J > 1 mA/ m. Figure 4.2.2 shows the differences in power dissipation for the read or write recorder mode for J < 1 mA/ m.

Linear current densities below 2 mA/μm are expected to be sufficient to successfully propagate bubbles in a prototype chip (values up to 1.5 mA/μm have been used in the present experimental studies). Using a return conductor twice as thick as each of the drive conductors (i.e. T = 1.5) and J = 2 mA/μm, the power dissipated is 0.25 watts. This means that in the recorder mode, (M) multiple areas could be simultaneously accessed (writing or reading data). Using a conservative power dissipation of 2 watts per chip this would allow M = 8 storage areas to be simultaneously run. Data rates with the (111) garnet would be 8 x 1.5 MHz or 12 MHz per chip. The (110) garnet with its much higher mobility would have

single chip data rates of 8 x ($\sim$20MHz) $\approx$ 160MHz. This would be a very strong benefit for high data rate recording and data handling. It is not unreasonable that up to 4 watts could be dissipated per chip. This corresponds to M = 16 and even higher single chip data rates.

### 4.2.2 Power Dissipation Operating in a Typical Worst Case Block Access Mode

This section repeats the analysis of the above section with the duty cycle numbers appropriate for a worst case block data access mode. In this case it is assumed that data is being recalled from a storage area and that each time the




Calculated power dissipation for 10 Mbit chip for two operating modes discussed in the text. The T parameter refers to the return conductor thickness: T = 1.0 => no return conductor, T = 1.5 => return conductor thickness is twice the propagation conductor thickness.

Figure 4.2.2

data block required to be read next is in the very worst possible location. The storage area cycles 751 times to place the desired data next to the I/O track. This set of bubbles is swapped into the I/O track. Then the I/O track and the storage area are cycled one step and another set of bubbles are swapped into the I/O track to complete the data block. Now the I/O track cycles times to read out the block of data. This entire process then repeats for the next block of data. Even though this is a very poor way to use a memory, it will provide a worst case power dissipation case for this study. Data calculated in the previous section will be used here with the appropriate duty cycles inserted for the power calculation for each segment of the memory.

Storage Area

Two adjacent storage areas cycle 751 times, transfer two bubbles from each storage loop, and then wait for 1662 cycles. Thus the duty cycle will be

$$d_s = \frac{752}{752 + 1662}$$

$$= 0.312$$

Using $d_\lambda = 0.75$ (as in the recorder model above) the storage area average power dissipation is given by

$$\langle P_s \rangle = d_s \times T \times d_\lambda \times J^2 \times (1618\mu m)^2 \left[ R_1 + R_2 \right]$$

$$= 0.93\ T\ J^2$$

with J in units of mA/micron.

I/O Track

The duty cycle for the I/O track is given by

$$d_{s,I/O} = \frac{1662}{752 + 1662} = 0.69$$

The average I/O track power dissipation is

$$\langle P_{I/O} \rangle = 0.69 \ \langle P_{I/O,\ rec} \rangle$$

$$= 0.69 \times T\ J^2 \times 0.037 \text{ watts}$$

$$= 0.026\ T\ J^2 \text{ watts.}$$

Swap Gates

The swap gates have a duty cycle given by

$$d_{SG} = \frac{2}{752 + 1662}$$

$$= 8.3 \times 10^{-4}$$

The average swap gate power is therefore given by

$$\langle P_{SG} \rangle = (8.3 \times 10^{-4})\ (0.04\ w)$$

$$= 3.3 \times 10^{-5} \text{ watts.}$$

Replicate Gates

The replicate gates have a duty cycle given by $d_{RG} = 0.5\ d_{SG}$
The average replicate power dissipation is given by

$$\langle P_{RG} \rangle = (0.5)\ (8.3 \times 10^{-4})\ (0.35w)$$

$$= 1.5 \times 10^{-4} \text{ watts.}$$

Detectors

The detector duty cycle is the same as the I/O track. Hence $d_{DET} = 0.69$. The average power dissipated will be

$$\langle P_{DET} \rangle = 0.69 \times 0.0062 \text{ w}$$

$$= 0.0043 \text{ watts.}$$

Discriminator

The discriminator duty cycle is 0.25 times the I/O track duty cycle. Thus

$$d_{DIS} = 0.25 \times 0.688$$

$$= 0.17$$

For the (110) garnet wall state coding scheme,

$$\langle P_{DIS} \rangle = (0.17)\ (3.2 \times 10^{-5} \text{ w})$$

$$= 5.4 \times 10^{-6} \text{ watts.}$$

As indicated earlier there does not exist a "double bubble/ single bubble" discriminator to model. Hence the (110) garnet discriminator is used here.

Generation

Assuming 200 ns pulses with the 666 ns propagation period, the average power dissipation in the generator is given by

$$\langle P_G \rangle = \frac{200}{666}\ (0.69)\ (0.0047 \text{ w})$$

$$= 9.7 \times 10^{-4} \text{ watts.}$$

Summary For The Worst Case Model

When writing or reading in this model the individual power contributions are:

Storage area -- $P_S = 0.93 \quad T\ J^2\ w$

I/O track -- $P_{I/O} = 0.026\ T\ J^2\ w$

Block swap gate -- $P_{SG} = 3.3 \times 10^{-5}\ w$

Generator -- $P_G = 9.7 \times 10^{-4}\ w$

Replicate Gate -- $P_{RG} = 1.5 \times 10^{-4}\ w$

Detectors -- $P_{DET} = 4.3 \times 10^{-3}\ w.$

As a result, $\langle P_{write} \rangle = 0.96 \quad T\ J^2\ w + 1.0 \times 10^{-3}\ w$ and

$$\langle P_{read} \rangle = 0.96\ T\ J^2\ w + 4.5 \times 10^{-3}\ w.$$

The first term of each of these two equations dominates the constant term for useful values of J. Hence the read and write power dissipation levels are shown as identical lines in Figure 4.2.2.

It should be noted here that the power calculations above have ignored power which would be lost in the bonding leads, bonding pads and control conductor lead ins. In addition, if an Al-Cu alloy is used for elements with an electromigration danger (the generators), the higher resistivity of Al-Cu as compared to Al will increase power dissipation in those elements. On the other hand, one could use gold conductors and reduce the power dissipation as well.

4.2.3 Thermal Effects

This section calculates some of the thermal effects (e.g. temperature rise, thermal conductance) for the 10 Mbit chip design with the power dissipation conditions calculated in the previous section. For this portion of the report it will be assumed that heat generated in the drive and control conductors is in direct thermal contact with the top surface of the garnet. Thus it will be the ability of the garnet to conduct and absorb heat which will be evaluated (in an attempt) to show that thermal effects would be reasonable. For the garnet modeling, the following constants will be used:

Thermal conductivity, $K = 0.08 \ \frac{\text{watt}}{\text{cm-}^{o}\text{C}}$

Specific heat, $c = 418 \ \frac{\text{j}}{\text{mole-deg}}$

Case 1 - One storage area in recorder mode

One storage area is made up of 831 storage loops with 752 bubbles each. The average power dissipation for one storage area, as calculated in the previous section, is given by

$$\langle P_{s,\ rec} \rangle = 3.6 \times 10^{-3}\ T\ J^2 \text{ watts.}$$

If we choose T = 1.5 and J = 1.5 mA/micron, then

$$P_{\text{one section}} = 3.6 \times 10^{-3} \times 1.5 \times (1.5)^2$$

$$= 1.22 \times 10^{-2} \text{ watts}$$

At a 1.5 MHz data rate it takes 0.83 s to fill one storage area. Thus the power dissipated in one storage area during filling is given by

$$Q = 1.22 \times 10^{-2} \text{ w} \times 0.83 \text{ s}$$

$$= 0.010 \text{ j}$$

If all of this energy goes into the garnet directly below the storage area, the resulting temperature increase can be calculated as follows:

$$\text{Volume of garnet, } V_G = 0.715 \text{ cm} \times 0.1618 \text{ cm} \times 0.05 \text{ cm}$$

$$= 5.8 \times 10^{-3} \text{ cm}^3$$

$$\text{mass of garnet, } m_G = \text{density} \times V_G$$

$$= 7 \frac{\text{gm}}{\text{cm}^3} \times 5.8 \times 10^{-3} \text{ cm}^3$$

$$= 4.1 \times 10^{-2} \text{ gm}$$

$$\Delta T = \frac{Q}{mc}$$

$$= \frac{0.010 \text{ j}}{\left[418 \frac{\text{j}}{\text{mole-deg}}\right] \quad 4.1 \times 10^{-2} \text{ gm} \quad \left[\frac{1}{739} \quad \frac{\text{mole}}{\text{gm}}\right]}$$

$$= 0.43 \ ^{\circ}\text{C}$$

This temperature rise is negligible.

The assumption that the electrical insulating layers will conduct the heat to the garnet can be checked by calculating the temperature difference across a layer for the power given above. Several insulating materials are listed below with their thermal conductivities:

| Material | Thermal conductivity, $K\left(\frac{\text{cal}}{\text{cm - sec - }^{\circ}\text{C}}\right)$ |
|---|---|
| borosilicate glass [14] | 0.003 |
| $SiO_2$ | 0.005 |
| polyimide | 0.0004 |

For a worst case calculation, a 0.5 micron layer of polyimide is used in the following calculation.

$$\Delta T = \frac{PL}{KA}$$

where P = power

L = thickness, and

A = area of layer.

$$\Delta T = \frac{1.22 \times 10^{-2} \text{ watts} \times 0.5 \times 10^{-4} \text{ cm} \left[\frac{1}{4.184} \frac{\text{cal}}{\text{j}}\right]}{\left[0.0004 \frac{\text{cal}}{\text{cm - sec - }^{\circ}\text{C}}\right] \times 0.1618 \text{ cm} \times 0.715 \text{ cm}}$$

$$= 3.2 \times 10^{-3} \, ^{\circ}\text{C}$$

This result is very acceptable, even with multiple layers.

Case 2 One storage area using the worst case access model

The power dissipated by one of the 18 storage areas for the worst case access mode (see section 4.2.2) is given by

$$\langle P_s \rangle = 0.93 \, T \, J^2.$$

Choosing T = 1.5 and the lineal current density, J = 1.5 mA/micron, the power dissipated is 3.1 watts. Because of the higher power level and the fact that this data access approach would not be used for a data recording mode, but rather would be more typical of accessing unrelated blocks of data, a steady state thermal conduction calculation is used to assess thermal effects. The propagation conductors dissipate heat at the top surface and it is assumed that a thermal conductor (part of the package) is in thermal contact with the bottom of the garnet substrate. A one dimensional model can be used to calculate the temperature difference, $\Delta T$, between the top and bottom surface of the garnet while 3.1 watts of power is conducted through the garnet. Calculating this temperature difference we get,

$$\Delta T = \frac{PL}{KA}$$

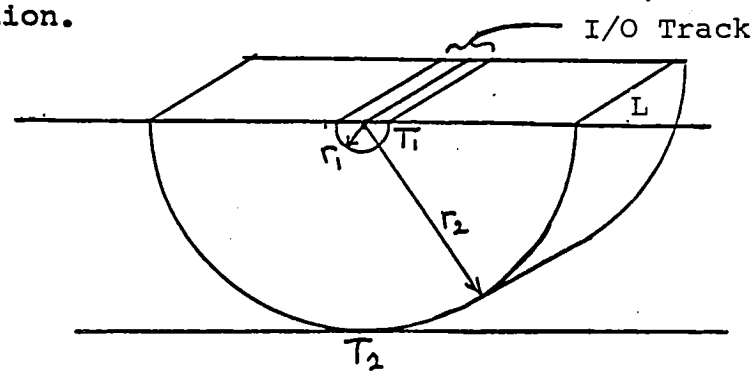
$$= \frac{(3.1 \text{ watt}) \, (0.05 \text{ cm})}{\left[0.08 \frac{\text{watt}}{\text{cm}^{\circ}\text{C}}\right] (0.1618 \text{ cm}) \, (0.715 \text{ cm})}$$

$$= 17.0 \, ^{\circ}\text{C}$$

This result may be acceptable. It is assumed that the package will dissipate heat adequately to prevent serious temperature rise if a storage area is used continuously.

Case 3 I/O track running continuously

A two dimensional heat flow model as shown in the sketch below is used to evaluate the effects of I/O track power dissipation.




The radius of the upper cylinder is equal to one-half of the I/O track width (10 microns). The radius ($r_2$ = 0.05 cm) of the larger cylinder is equal to the total garnet thickness (magnetic epi layer plus substrate). A temperature difference, $\Delta T = T_2 - T_1$ exists between $r_1$ and $r_2$. The cylinder length, L = 0.715 cm, is the I/O track length and the 0.125 watts of power are dissipated by the I/O track.

The equation for heat conduction for this geometry is

$$\frac{dQ}{dt} = P = \frac{1}{2} \frac{\Delta T \times 2\pi K L}{\ln\left[\frac{r_2}{r_1}\right]}$$

where the leading 1/2 comes from the use of 1/2 of a cylinder.

Solving for $\Delta T$ gives

$$\Delta T = \frac{2\,P\,\ln\left[\frac{r_2}{r_1}\right]}{2\pi KL}$$

$$= \frac{2(0.125\ w)\ \ln\left[\frac{0.05\ cm}{10 \times 10^{-4}\ cm}\right]}{2\pi\left[0.08\ \frac{watt}{cm\ ^{o}C}\right]\ 0.715\ cm}$$

$$= 2.72\ ^{o}C$$

This result would indicate that the I/O track heat should satisfactorily be conducted away from the I/O track area.

A calculation of the heat flow rate through an insulating layer under the I/O track also shows reasonable behavior as shown below. Using the same material, thickness, etc. as for the storage area we see that:

$$\Delta T = \frac{PL}{KA}$$

$$\Delta T = \frac{(0.125\ w)\ (0.5 \times 10^{-4}\ cm)\left[\frac{1\ cal}{4.18\ j}\right]}{\left[0.0004\ \frac{cal}{cm - sec - ^{o}C}\right]\ (0.715\ cm)\ (20 \times 10^{-4} cm)}$$

$$= 2.61\ ^{o}C$$

Case 4 Generators

The last thermal calculation is for heat dissipated at the generators to be conducted away. The model to be used here will be radial three dimensional heat flow in one-half of a sphere. The equation for thermal conduction for 1/2 of a sphere is

$$P = \frac{dQ}{dt} = \frac{\Delta T \times 4\pi K\, r_2\, r_1}{r_2 - r_1}$$

Choosing $r_1$ = 5 microns (this is the weakest part of this model), $r_2$ = 0.05 cm, K = 0.08 w/cm - $^{o}$C for garnet, and $P_G$ = 0.00097 watts, T can be calculated. This value of $P_G$ is for the recorder mode which is the largest generator power level of the models shown.

$$\Delta T = \frac{P\,(r_2 - r_1)}{4\pi K\, r_2\, r_1}$$

$$= \frac{(9.7 \times 10^{-4} w)\quad \left[(0.05\ cm) - (5 \times 10^{-4}\ cm)\right]}{4\pi\ (0.08\ w/cm - {}^{o}C)\ (0.05\ cm)\ (5 \times 10^{-4}\ cm)}$$

$$= 1.91\ {}^{o}C$$

This result appears to indicate that even the generator will not create excessive temperatures.

## 4.3 Discussion of Device Designs and Packaging

This section will briefly discuss the implications of the designs presented, the power/thermal modeling, and some benefits of the self-structured, current access approach from a chip or board point of view.

The two device designs, Figure 4.1.9 and Figure 4.1.15 indicate possible goal or target devices for the evaluation or further development of this technology.

The Figure 4.1.15 device in particular appears to take good advantage of the benefits of the self-structured approach. The ability to asynchronously run storage areas and I/O tracks independently from each other and one another provides considerable flexibility in how the device is controlled. For example, data can be pre-queued in one storage area while being read out from another. A similar approach can be used for writing data. Overall, this can reduce the effective access time or wait time to zero for reading data from or writing data to specific areas in storage. Alternately, by using the multiple detectors and I/O read tracks to cache regularly used data, a small, reasonably flexible, high speed secondary cache storage memory can be implemented.

The Figure 4.1.15 device also takes maximum advantage of the defect tolerant aspects of the self-structuring by having no redundant loops or areas while still potentially having good fabrication yield. This provides far better utilization of die area and effectively increases the data rates compared to a device which has redundant loops which result in some percentage of useless data being moved in and out on the I/O tracks.

An important benefit of the self-structuring is the increase in density obtained for a given bubble size and material $4\pi M$ and also for a given maximum current density in control conductors. The current densities which can be tolerated in borderline components such as generators and replicate gates define a maximum $4\pi M$ and thus a minimum bubble size which can be accommodated. Third dimension or vertical scaling of conductor thicknesses also define a minimum bubble size in a practical device. The same limitations on bubble size hold for self-structured devices as well, however, for a given bubble size, the self-structured device has a factor of four or more greater data density and device capacity. In practice, the minimum convenient bubble size is in the range of 1.5 - 2.0 microns. This means that the self-structured device can achieve a significant increase in data density in a current access device and do it with optical lithography.

A big advantage of the current aperture-accessed bubble memory is the architectural flexibility which is available. No X or Y drive coils are necessary (as required in field-accessed devices). Thus the size or shape of the chip can be varied as desired. It may be appropriate to use non-square chip shapes to maximize the memory density on available board space and/or to keep costs down. The elimination of the need for X or Y drive coils will also simplify device construction and reduce costs.

One area of concern for bubble devices in general has been whether they could meet wider temperature range specifications than have been available in currently available bubble devices. While this contract has not been involved in wider temperature range efforts, it should be noted that recent work has developed a wide temperature technology for use with conventional, field-accessed bubble devices [10]. These developments primarily involve the tailoring of magnetic garnet material and the thermal properties of the bias magnets. Those efforts should be directly applicable to the current aperture-accessed devices described here.

## Packaging

Detailed work on device packaging was not included in the tasks for this project. However, some of the analysis that was done (e.g. chip size and power dissipation) required a look at packaging to be sure that potential chip layouts could be accommodated in realistic packages.

Power dissipation calculations for the 10 Mbit prototype (Section 4.2) indicate that power levels well under one watt would be required for the recorder mode and levels under four watts would be dissipated in the worst case access mode (refer to Figure 4.2.2). Conventional permalloy, field-accessed (1 to 4 Mbit) bubble devices dissipate over 5 watts in their active mode in a nominal one and one-half inch squared package [11]. Thus the power dissipation design requirements for the 10 Mbit self-structured chip will be within the abilities of current packaging technology.

There exists at the present time sufficient packaging technology to handle current aperture-access devices as described in this report. Further work in packaging should be carried on in parallel with continued development of the self-structrued, current aperture-access bubble memory.

## 5.0 Summary

The goal of this research project has been to evaluate the dual conductor, current access, self-structured, bubble memory concept as a potential memory device. This effort has included; (1) experimental design, fabrication and testing of test circuits, (2) theoretical studies of various device geometries, and (3) comparison studies of non-volatile memory devices and systems. No fundamental technical reasons for not continuing this technology development have been found.

There are yet a number of fundamental tasks to be achieved before a prototype device can be built. The primary task ahead is to integrate data coding into the propagation and gating schemes developed under this contract.

As a result of this study it is the conclusion of the authors that self-structured magnetic bubble memory is a viable technology. The primary advantages remain those which were outlined in the initial proposal and earlier reports;

1. Increased device data density by a factor of four over non-self-structured bubble memories.

2. Defect tolerance -- This has been demonstrated in this study.

3. Higher data rates -- The current access propagation method, not limited by field coils, can move bubbles fast enough to achieve 1.5 MHz data rates in (111) garnets. Orthorhombic garnets offer considerably higher data rates.

The current plan of the Sperry Advanced Materials and Devices Corporate Technology Center is to continue this work using Corporate research and development monies. This effort is currently working toward the following goals;

1. To integrate data coding into the device structures.

2. To build a simplified, or partially populated, device, and

3. To work toward the eight storage area device shown in Figure 4.1.13.

# Appendix A - Fabricating Circuitry Over Ion-Machined Garnet Barrier Steps

## A.1 Introduction:

This appendix covers the approaches and techniques used in fabricating apertured conductor circuitry over ion-machined barrier steps in garnet films. The discussion is broken into three topics: polyimide planarizing (Figure 3.5.4a), elimination of milling redeposition knife edges (Figure 3.5.4a and b), and profiled barrier steps (Figure 3.5.4c).

The difficulty addressed with each approach is fabricating electrically continuous thin film layers over ion-machined vertical steps in the garnet. These steps must be abrupt from the horizontal perspective of a bubble diameter.

## A.2 Polyimide Planarizing

The polyimide (PI) approach uses ion-machined barriers with $90^{o}$ steps which are covered with spun-on PI to give a planar surface for subsequent processing. Various polyimides [13] were used in the fabrication of smoothing/insulating layers for some of the test bubble devices. An organosilane adhesion promoter [17] was prepared as follows:

Mix
95. ml methanol
5. ml water
0.5 ml adhesion promoter

Let stand 12 hours

Filter (0.2 μm) at point of use.

The adhesion promoter solution was applied to the substrate in the same manner as when coating with photoresist. After this the spinning surface was sprayed with methanol. The polyimide was then applied to the substrate directly from a squeeze bottle - being spun on at 8000 RPM (without dilution). This gave a coating thickness of 800 nm. The coated substrates were placed on a preheated hot plate 120-135$^{o}$C for one-half hour. If vias were required the PI was coated with positive photoresist (PR). The vias in the PI were then etched with

an alkaline developer [18]. The PR was removed with acetone and the substrate was returned to the hot plate. The temperature was then increased from 135°C to 370°C at a temperature of ∿6°/min. Next, the substrate was transferred to a vacuum oven and held at a maximum temperature of 400-405°C for 10 min. Once removed from the vacuum oven, the substrate was stored in a desiccator if not loaded directly into a vacuum system. This was done in order to avoid water absorption.

Water absorption has been identified as a potential problem in PI processing. Initially the Al-Cu conductor was deposited directly over the PI. In subsequent high temperature processing steps, e.g., NiFe deposition and the curing or imidization of succeeding PI layers, the conductor "blistered." The blisters never appeared in apertured areas or narrow conductors but did in pad areas and where the conductors were wide or fanned out to pads over PI. This suggested that the PI was degassing and that outgassing could occur into covered areas without affecting the adhesion of apertured or narrow conductors.

To reduce water absorption (in addition to storing in a desiccator between process steps) and outgassing in subsequent processing steps, the PI was coated with 2000 Å of sputtered glass [14] prior to deposition of the first conductor layer. Also, the use of PI as a conformal coating was limited to the garnet (barriers). Sputtered glass also served as the dielectric between conductors.

Bonding was unsuccessful when the conductor pad had been deposited and etched on top of only a few thousand angstroms of glass coating over the PI. Attempts to bond resulted in perforation of the pad and the glass. However, bonding was successful when the pad was directly on garnet or directly on glass over garnet. Also, bonding was successful when a thick dielectric layer (e.g., 1.0 μm glass) was interposed between the PI and the bonding pad.

Vias are easily etched in partially cured PI which permits deposition and definition of the bonding pad directly on the garnet, thereby eliminating any deleterious effect the PI might have had on the bonding process.

A complete process outline for PI planarized bubble device fabrication is:

Barrier - Separation Layer

1. Barrier photolithography
2. Ion-Mill
3. Polyimide conformal coating 800.0 nm
4. Sputter glass 200.0 nm

1st Drive Conductor

| | | |
|---|---|---|
| 5. | Deposit Al(Cu)/Cr | 350/35 nm |
| 6. | Conductor photolithography | |
| 7. | Ion-Mill | |

Dielectric and Vias

| | | |
|---|---|---|
| 8. | Sputter glass | 1000 nm |
| 9. | Via photolithography | |
| 10. | Etch vias, etch Cr | |

2nd Drive Conductor

| | | |
|---|---|---|
| 11. | Sputter Al | 400 nm |
| 12. | Vapor deposit Cr | 35 nm |
| 13. | Conductor photolithography | |
| 14. | Ion-Mill | |

Dielectric

| | | |
|---|---|---|
| 15. | Sputter glass | 1000 nm |

Detector

| | | |
|---|---|---|
| 16. | Vapor deposit NiFe | 35 nm |
| 17. | Detector photolithography | |
| 18. | Ion-Mill | |

Control Conductor

| | | |
|---|---|---|
| 19. | Sputter Al | 450 nm |
| 20. | Conductor photolithography | |
| 21. | Ion-Mill almost to completion | |
| 22. | Finish with wet chem etch | |

Vias

| | |
|---|---|
| 23. | Via photolithography to 1st & 2nd drive conductors |
| 24. | Etch vias, etch Cr |

Test Packaging

| | |
|---|---|
| 25. | Dice |
| 26. | Mount on board |
| 27. | Bond |

## A.3 Redeposition Elimination

An initial difficulty encountered when ion-machining barrier steps in the garnet films was redeposition of the garnet material on the edge of the surrounding (defining) photo-resist. This resulted in garnet vertical knife edges after

removal of the photoresist. Figure A.1 shows a cross-section of a completed propagation loop with mesa barriers. The cross-section thickness profile was measured using a profilometer with a 12.5μm diameter stylus. The path of the measurement is indicated in Figure A.2. What is significant is the 200 nm redeposition peaks (2 + 8 in Figure A.1) which are present after milling 200 nm into the garnet to form the barrier steps and depositing 300 nm SiO, 350 nm Al-Cu, 400 nm glass, and 450 nm of Al-Cu. This circuit didn't function properly as the Al-Cu conductors were not continuous across the knife edges.

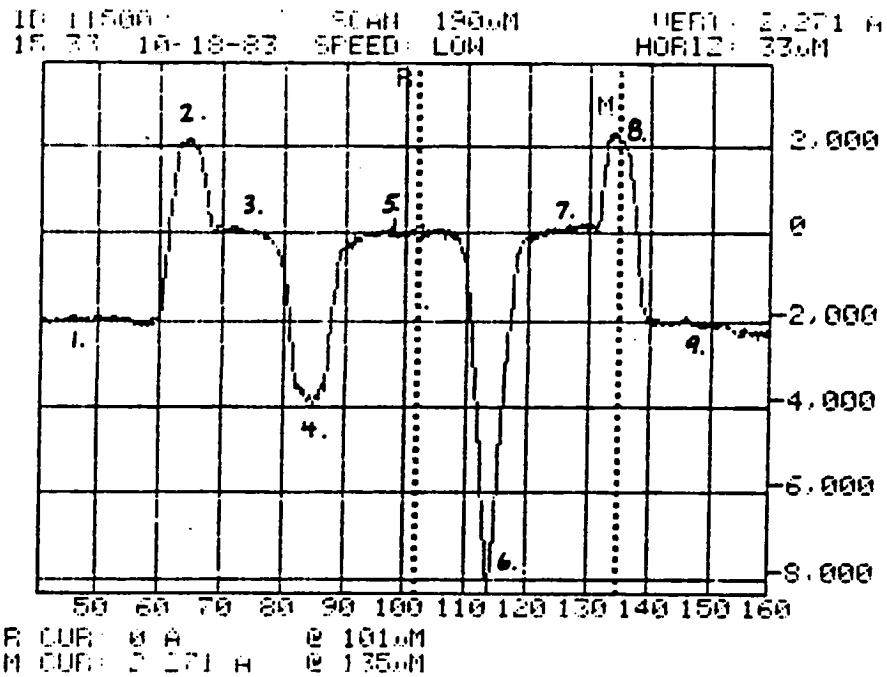
The redeposition problem was resolved by substituting a lower viscosity resit in place of the previously used photoresist [19]. The lower viscosity photoresists have a lower percentage of solids resulting in a thinner resist coating, (typically 0.5μm. The thicker resist coating (1.5μm) in this instance served no useful purpose but did enhance redeposition. Garnets were milled in an ion etcher with the ion beam normal to the substrate surface, so as to obtain steep, well-defined walls and, therefore, sharp energy wells for bubble control.

Figure A.3 shows a profile of a recess loop without the redeposition. The clean milling edges obtained helped improve conductor crossing continuity. Elimination of the redeposition, however, didn't completely eliminate the conductor continuity problems. The no-redeposition approach was also used for PI planarizing devices covered in Section A.2.

## A.4 Profiled Barrier Steps

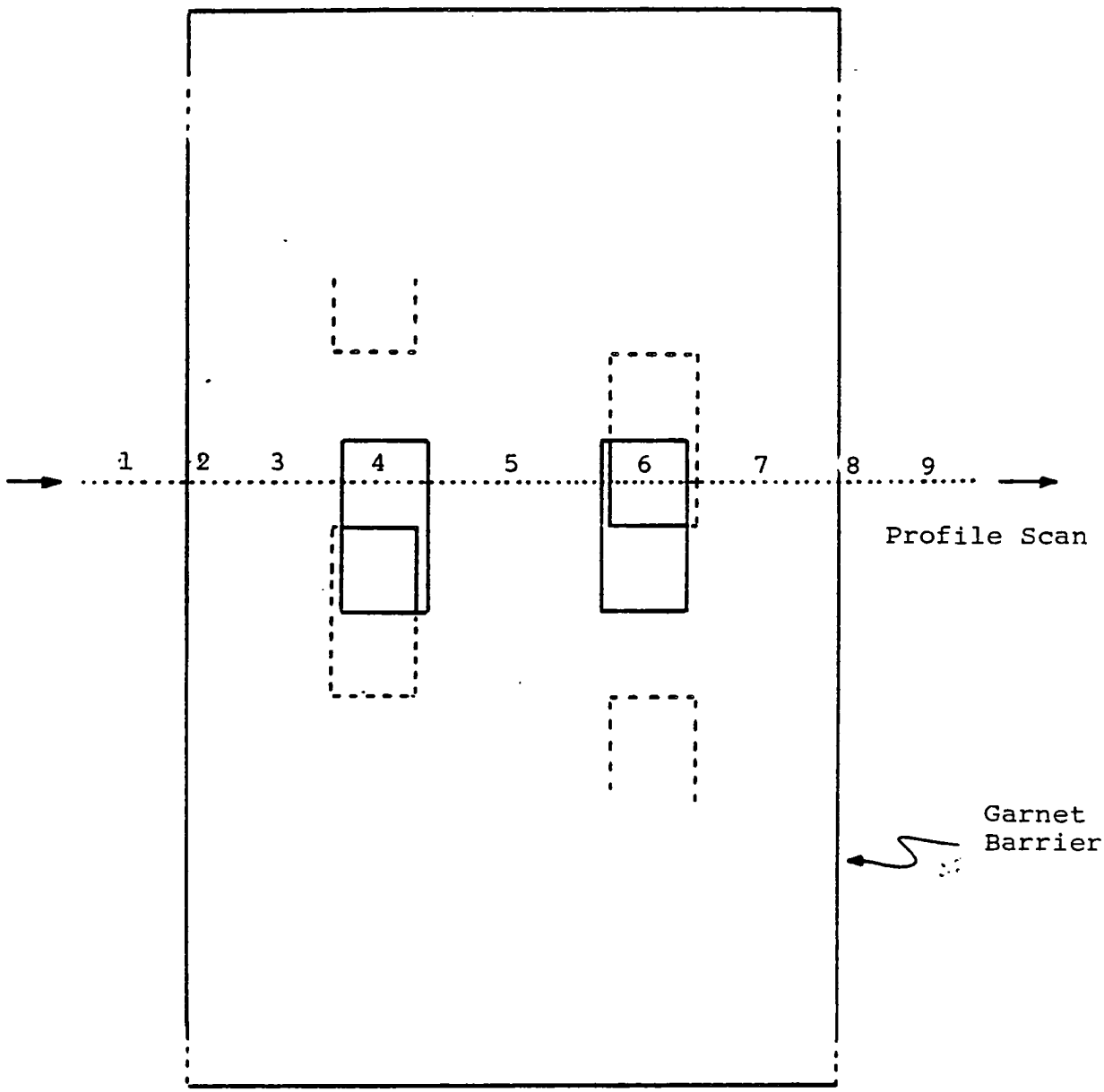
Resist profiling was explored as another possible solution to the redeposition problem and also as a means for obtaining sloped barrier steps for better conductor continuity. In this approach, after developing the barrier patterns in the photoresist on the garnet, the sample is given a post development bake. During this bake, in the 90°C - 120°C range, surface tension of the photoresist rounds the edges exposed in the developed pattern.

This rounding, or profiling, of the photoresist has three major effects on the ion-milled barriers. First, redeposition is eliminated since a vertical wall of photoresist is no longer present to capture material, and if any material is redeposited onto the profiled photoresist, it is exposed to the ion beam. Second, the taper of the profiled photoresist may be replicated in the milled pattern. Third, as a result of this replication, the milled pattern does not exactly match the mask dimensions. For example, in a recess barrier



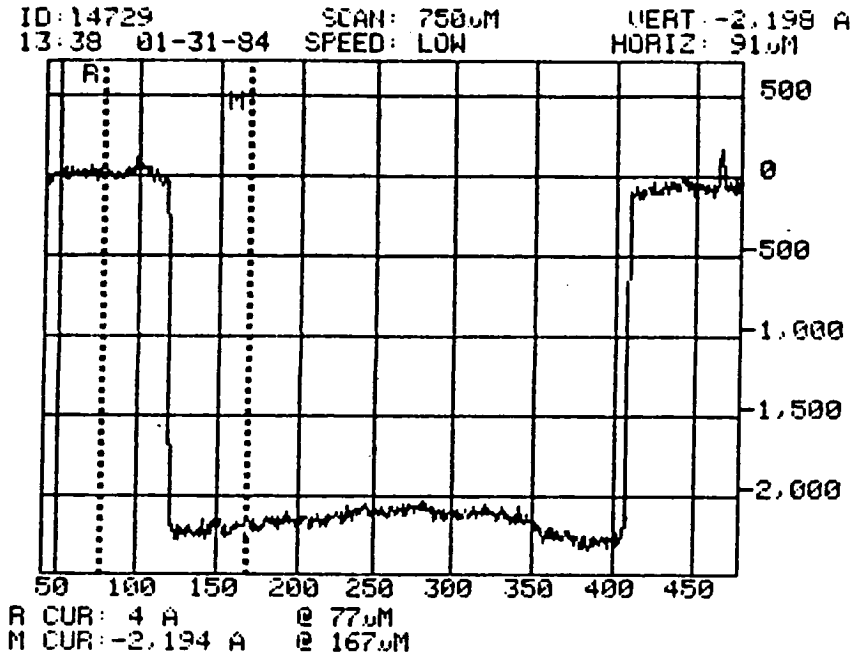

Thickness profile of a Chip II mesa showing redeposition knife edges.

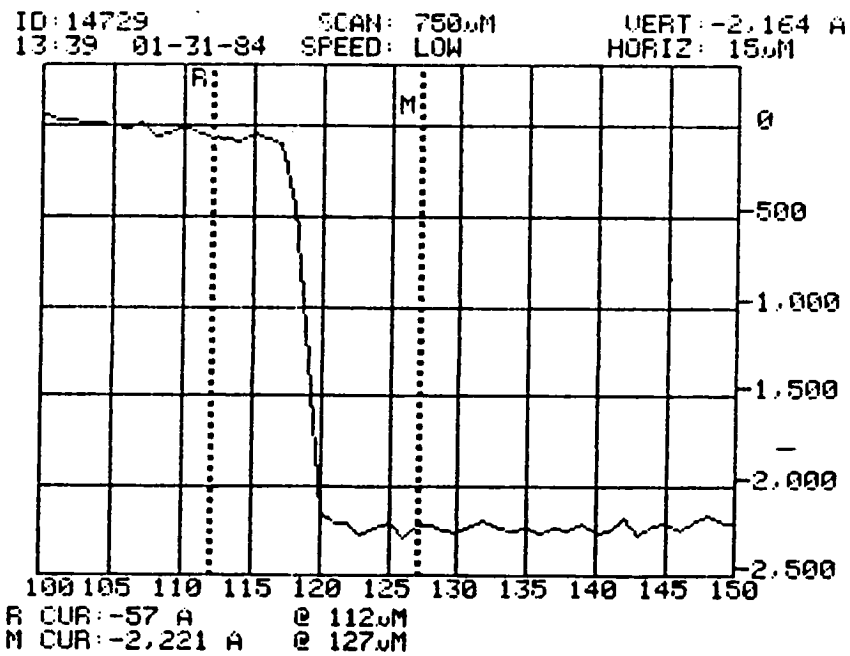
Figure A.1




Profile track across Chip II circuit.

Figure A.2




Thickness profile of a recess barrier showing the elimination of redeposition knife edges.

Figure A.3

loop, the barrier edge is effectively moved outwards resulting in its being mispositioned if the effect is not anticipated in the mask design.

This resist or profiling approach was successful at eliminating redeposition. Again, measurements confirming this were made with a profilometer. Using the thinner photoresist coating as described in Section A.3, however, is more convenient if the redeposition problem is the only concern (such as when PI overcoating) and if the barrier step is small enough (<0.4μ). For larger barrier steps, a thicker photoresist coating is necessary to maintain coverage during the longer ion-machining interval. In this case, profiling the resist to eliminate redeposition is the preferred approach. A number of samples were fabricated with 1.0μm barrier steps using photoresist at 1.2μm thickness with a 1/2 hour profile bake at 90°C. This resulted in clean, vertical barrier steps.

Resist profiling at higher temperatures gave more tapered photoresist edges which were replicated into the garnet during ion-machining. Both mechanical profiling and SEM photo approaches were tried for characterizing the garnet profiling. The profilometer approach was unsuccessful due to the large stylus (12.5μm diameter) available. Obtaining the smaller sized stylus available (0.5 - 1.0μm would make this a good approach. The SEM photos provided some qualitative characterization but were not used extensively. The best qualitative approach was to use relatively large barrier steps (0.4 - 0.5μm and observe the broadening of the barrier edge in an optical microscope. In this way, it could be observed that some tapering had been obtained in the garnet although quantitative slope or profile-shape data was not obtained. Completed test circuits of chip II which were built with these barriers worked well electrically with barrier step heights of 200 nm. The barrier performance however was marginal. Larger barriers step heights gave better barrier behavior but poorer conductor performance. Overall, this approach has promise but requires quantitative barrier profile characterization with a profilometer with a small diameter stylus.

## A.5 Summary

For final test sample fabrication, the approach used was to eliminate ion-machining redeposition with either thin resist for shallow barrier or thicker resist with low temperature profiling for larger barrier steps. In both cases, vertical garnet steps were desired. They were covered with a planarizing coating of polyimide and glass.

# MEMORY TECHNOLOGY OVERVIEW

David S. Lo

SPERRY CORPORATION

April 1984

This Memory Technology Overview was prepared for NASA under contract NAS1-16911.

The writer acknowledges the valuable suggestions of Paul J. Hayes, project monitor at the NASA Langley Research Center.

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## PREFACE

This report is an overview of memory technologies at the device level. It presents various types of memories as well as technologies. Although every effort has been made to make this report as accurate and current as possible, it is in no way claimed to be complete. It is intended as a general reference.

As an introduction, various types of past, present, and future semiconductor, magnetic, and optical memories are briefly described and compared at the device level. Then, requirements and selection of suitable memories for military and space applications are presented. Finally, five memories are discussed with regard to operating principle, speed, density, data retention, endurance, power, cost, temperature, radiation resistance, advantages, disadvantages, and applications: complementary metal–oxide–semiconductor (CMOS) with battery, floating gate electrically erasable programmable read–only memory (EEPROM), metal–nitride–oxide–semiconductor (MNOS), magnetic bubble, and magnetic cross–tie.

In addition to the benefits derived from the listed references, the materials presented have been greatly influenced by the Twenty–eighth Annual International Magnetics Conference held in Philadelphia, Pennsylvania, April 1983; the Sixth IEEE Nonvolatile Semiconductor Memory Workshop held in Vail, Colorado August 1983; and the Large Scale Memories Symposium held in Willow Grove, Pennsylvania, September 1983. Thanks and appreciation are also due to many people both within and outside Sperry Corporation for their support and contributions.

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Eagan, Minnesota
April 1984

David S. Lo

# SECTION 1

# INTRODUCTION

In the past 30 years, memory technology has made enormous advances and is continuing its advancement at a fast pace. Various types of memories have been developed and many new ones are in the research and development stage. The list in Table 1 is the best evidence.

TABLE 1. MEMORIES IN PAST, PRESENT AND FUTURE

<table>
<tr><td colspan="2">MEMORY WITH MOVING PARTS<br>Magnetic Drum<br>Magnetic Tape (Optical Tape)<br>Magnetic Disk (Fixed or Moving Head, Rigid or Floppy Disk, Vertical Recording)<br>Optical Disk (Read Only, Read and Write, Stylus or Laser Head, Jukebox)</td></tr>
<tr><td>MEMORY WITH NO MOVING PARTS, SOLID STATE<br>SEMICONDUCTOR<br>Volatile<br>Dynamic Random Access Memory (DRAM)<br>Static Random Access Memory (SRAM)<br>Pseudo SRAM<br><br>Nonvolatile<br>Read Only Memory (ROM)<br>Programmable Read Only Memory (PROM)<br>Erasable Programmable Read Only Memory (EPROM)<br>Electrically Erasable Programmable Read Only Memory (EEPROM)<br>Nonvolatile Random Access Memory (NVRAM)<br>Combination Read-only and Electrically Erasable Programmable Read-only Memory (CREEM)<br>Metal-Nitride-Oxide-Semiconductor (MNOS), Silicon-Nitride-Oxide-Silicon (SNOS)<br>Complementary Metal-Oxide-Semiconductor (CMOS) with Battery</td><td>MAGNETIC<br>Core<br>Film (Single or Mated, Domain)<br>Wire<br>Bubble (Conventional, Field or Current Access, Self-structured, Vertical Bloch Line)<br>Cross Tie<br><br>OTHERS<br>Electron Beam Addressable<br>Magnetic Domain Tip Propagation<br>Ferroelectric<br>Sonic Film<br>Woven Plated-Wire<br>Optical (Read Only, Read and Write, Holographic, Bit Recording)<br>Charge-Coupled Devices (CCD)<br>Gallium Arsenide (GaAs)<br>Josephson Junctions (Super Conductor)<br>Ovonic (Ovshinsky)</td></tr>
</table>

Memory is a multi-disciplinary technology spanning magnetics, optics, and semiconductors. Memory manufacturing involves chemistry, ceramic, metallurgy, optic, vacuum, laser, crystallography, electronic, and thin film technologies. Each type of memory is based on a different operating principle and has its own merits. For example, optical erasable memory uses the magneto-optical effect and is randomly accessible while the charge-coupled device uses charge packets to represent data and is basically a serial access shift register. It is difficult to make a rigorous comparison on the same basis. To illustrate several selected types of memories from a user's point of view, a cost per bit versus access time diagram is shown in Figure 1. The cost per bit increases for faster access time. However, the readout data rates for these memories all center around 1 MHz. This demonstrates the difficulty in comparing memory technologies. The other features of each memory could be similar or drastically different. In addition to cost, access time, and data rate, the capacity, mean time between failures, error rate, operating temperature range, radiation tolerance, power consumption, data retention, durability, cycle time, write time, erase time, and data organization format should also be considered. A single memory that is cost effective and suitable for all applications probably will never be found. Selection of memory depends mainly on the specific applications and is a process of matching and compromising characteristics.

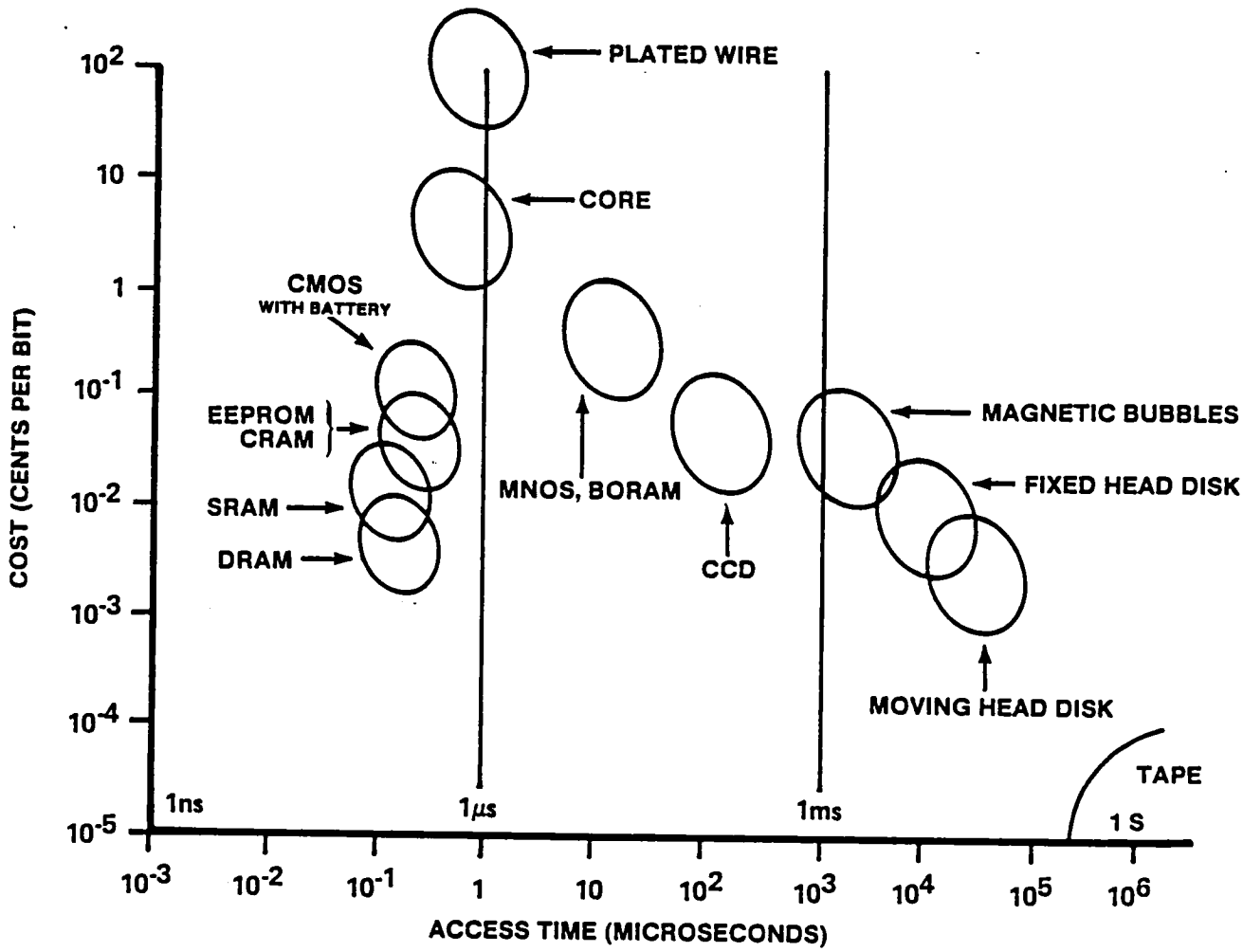



FIGURE 1. MEMORY TECHNOLOGY COMPARISON

# SECTION 2

# DESCRIPTION

## 2.1 MEMORY WITH MOVING PARTS

In spite of the maintenance and catastrophic mechanical failure problems associated with devices having moving parts, drum, tape, and disk memories are still widely used for their large capacity, moderate data rate, and low cost. Recent developments in vertical magnetic recording and optical disk further strengthen their competitive positions in memory technology.

### 2.1.1 Magnetic Drum

The bearing and the installation of the drum are usually ruggedized to sustain shock and vibration for high reliability, long lifetime (over 100,000 hours), and low error rate ($10^{-13}$). Drums can be sealed to reduce head crashes and keep out dust to minimize abrasion and errors. It is difficult to remove and store the drum. Because of the cylindrical symmetry of the drum, the linear surface velocity of all the data tracks are the same. The drum produces uniform air currents under the flying heads, making head design easier. The data access time can be shortened by increasing the drum rotating speed (e.g. 24,000 rpm) and using multiple heads. The drum memory is nonvolatile and radiation resistant. Drums offer access times as low as 8 milliseconds, capacities of 59 million bits, and bit transfer rate of 2 megahertz per second for each read-write amplifier. Drums have been used for program storage and multipurpose military programs such as Airborne Warning and Control System, B-1, P-3C, S-3A, BQQ-5, and BQQ-6.

### 2.1.2 Magnetic Tape

The increase in computer capacity and throughput created a need for storing and processing large quantities of high speed data. A magnetic tape system is a good candidate to fulfill this need. For example, it can be used to store a large quantity of digitized imaging and graphical data from a high-speed source for later processing.

Modern tape systems have a very high data transfer rate (up to 1 gigabit per second), a very dense storage (up to 100 kilobits per inch per track or 30 megabits per square inch), and a very large capacity (up to $10^{12}$ bits per reel). The tape system is a mature, low cost, low risk technology and can be easily adapted to new improvements in tapes and heads. However, the tape systems are serial accessed. The data access time can be as long as several hundreds of seconds depending on the reel length and tape speed. This mode of operation leads to inflexibility in computer interface and low performance. In addition, the tapes are fragile, have a limited temperature range, and require special attention for handling and storing. Electro-mechanical parts require scheduled maintenance. These difficulties result in a low reliability: an error rate of $1x10^{-10}$ now and $1x10^{-12}$ in the near future. Trends of development are cartridge loading such as the newly unveiled IBM 3480 tape drive and increase of recording density to 500 tracks per inch and 150 kilobits per inch.

Magnetic tape recording is nonvolatile, can be used for archival storage of historical data, a backup for other types of large capacity memories, and a means for transporting data between systems.

Optical tape systems have been demonstrated but are not as popular as the magnetic tape systems.

### 2.1.3 Magnetic Disk

Magnetic recording is a mature technology. Magnetic disk memories have been the mainstay of data storage for many years. The stored data are nonvolatile and can be written and read an unlimited number of times. For the past 25 years the key performance parameters of the magnetic disk have steadily improved, about 3.5 orders of magnitude in areal density, two orders of magnitude in access time, and 2.5 orders of magnitude in data rate.

The current IBM 3380 disk achieves a density of $1.2 \times 10^7$ bits per square inch, an access time of 16 milliseconds, and a data rate of 3 megabytes per second. Future improvements are anticipated but the density is not expected to exceed $10^8$ bits per square inch.

Recent research focused on vertical recording because of its high density due to the reduced self-demagnetization. A density of $10^8$ to $10^9$ bits per square inch is achievable. A flexible disk drive using vertical recording based on a cobalt-chromium recording medium is being developed by Toshiba. They plan to produce a 3 1/2-inch disk with 3 megabytes per side in 2 years.

### 2.1.4 Optical Disk

About 20 companies in the United States, Japan, the Netherlands, and France are actively engaged in optical disk development. Recent research makes it feasible to store nonerasable data of 10 gigabits per side for a 12-inch diameter disk, a corrected error rate of 1 bit in $10^8$ to $10^{12}$ bits, a read and write rate of 5 megabits per second per single channel, a random access time of 100 to 500 milliseconds, and an archival life of 10 years. The characteristics compare favorably to magnetic disks in capacity (bit-packing density) and archival time. In addition, the optical disk costs less and does not have many of the mechanical and storage problems of magnetic media. A 10-gigabit optical disk is now selling at about $250. This may reduce to $100 when the market is fully realized. The cost of a drive system is projected to be $10,000. The nonerasable optical disk can replace the write-once, unlimited-read market (presently occupied by the magnetic disk and tape) in the next few years.

The nonerasable disks have various sizes (3- to 14-inch diameters), structures (air sandwich or in-contact overcoat), substrates (aluminum, plastic, or glass), and single or multi-layer proprietary recording materials. Two recording techniques are generally used: one creating a small hole, the other changing the crystalline structure of the recording material. Both use a modulated laser beam for writing. Playback also uses a laser to detect the difference in reflectivity or optical interference for distinguishing data bits.

The optical disks have been arranged in a jukebox system to increase capacity and reduce the disk access time. For example: RCA is fabricating a jukebox system storing $10^{13}$ bits on 128 nonerasable disks with a disk retrieval time of 5 seconds and a corrected bit error rate of 1 in $10^8$. The record and read rates will be 40 Mbits per second per channel.

Prototype and experimental erasable optical disks are being developed. Disk sizes range from 2 to 8 inches with various recording materials such as tellurium alloy (Panasonic) for phase change recording and rare-earth transition-metal alloy (such as Philips, KDD, Sharp, NHK, 3M, and Xerox) for magneto-optical recording. Lasers are used for read, write, and erase functions.

A tellurium alloy changes its reflectivity between amorphous and crystalline phases. However, the alloy only allows up to 1 million phase changes or write-erase operations. When the medium is prepared in the crystalline phase, a short laser pulse will change the heated spot to amorphous phase. A long laser pulse will revert the heated spot to crystalline phase. The write and erase operation, as described, will cause slight degradation in the readout signal-to-noise ratio. A loss of 4 dB was reported after $10^5$ write-erase cycles.

The gadolinium-terbium-iron amorphous rare-earth transition-metal alloy used by Philips is a magneto-optical data storage medium. A data bit is represented by orientation of the magnetization in a small area. Writing is done by simultaneously heating via laser the data bit area to above the Curie temperature of the alloy and applying a magnetic field. Since thermomagnetic writing is nondestructive, the erase-write cycle is unlimited. Reading is done by the Faraday (or the Kerr) magneto-optical effect. A capacity of 10 megabytes on a 2-inch diameter disk has been achieved. This system will have a write time of 3 microseconds per bit, a read time of 250 kbits per second, and an access time of 50 milliseconds. These characteristics are better than those of magnetic floppy disks. Sony and KDD use terbium-iron-cobalt alloy for magneto-optical recording and demonstrate a read or write rate of 9 MHz and a signal-to-noise ratio of 52 dB. Using an 8-inch diameter disk, a capacity of 600 megabytes per side has been demonstrated. Many promising exploratory results have been reported that should lead to the introduction of erasable optical disks in the 1986 to 1988 time period.

## 2.2 MEMORY WITH NO MOVING PARTS, SOLID STATE

### 2.2.1 Semiconductor

The days of using discrete transistors and tunnel diodes as memory elements are long gone. The present semiconductor memories are all integrated circuits. Owing to the growing interest in personal computers and video games, the semiconductor memory enjoyed a tremendous growth in recent years. Functionally, semiconductor memories are categorized as both volatile and nonvolatile.

#### 2.2.1.1 Volatile Memory

##### 2.2.1.1.1 Dynamic Random Access Memory

Each dynamic random access memory (DRAM) cell is composed to two devices: one transistor and one capacitor. The cell structure is simple and small so that low cost and high chip capacity can be achieved. A 64K chip currently sells at $6 for a single unit; that is equivalent to 0.01¢ per bit. For large quantities, 0.004 to 0.005¢ per bit is possible. The 256K chips are now becoming available. Furthermore, recent announcements made by IBM indicate that experimental versions of 512K and 1M chips have been demonstrated. It looks as if the 1M chip goal might be reached by 1987. The DRAM are very fast with read or write in the 100- to 200-nanosecond range. The major drawback of DRAM is that data bits are stored as charges in the capacitors. The capacitor requires refresh or recharge in a period of milliseconds to prevent charge leakage and thus loss of data. The refresh must be carried out between read and write operations and requires additional circuitry. Figure 2 shows the history and trends of the various density DRAM.

##### 2.2.1.1.2 Static RAM

The static random access memory (SRAM) requires six devices for each memory cell: four transistors and two resistors. The basic cell size of a SRAM is larger than that of a DRAM. The SRAM chip capacity is smaller than DRAM, usually by a factor of four. Presently, only 16K and 64K chips are available. The 256K chips are expected by 1987. The 16K SRAM sells at $10 per chip, which is equivalent to 0.06¢ per bit. For large quantities, 0.02¢ to 0.03¢ per bit is possible. SRAM is also fast for read or write in the 100- to 200-nanosecond range. Specially designed small capacity 16K by 1-bit and 4K by 4-bit SRAM are as fast as 35 to 45 nanoseconds for commercial temperatures, 55 to 70 nanoseconds for the military temperature range. For special military use, conventional complementary metal-oxide-semiconductor (CMOS) transistors serve as resistors in place of polysilicon load resistors whose resistance decreases as temperature increases. This is done at the expense of cell size. Static RAM do not need refreshing, so data are retained as long as the power is connected. SRAM are therefore easier to use because there is no refresh circuitry. SRAM cells can be high-speed bipolar emitter coupled logic or transistor-transistor logic (Fujitsu: 1K device, access time 7 nanoseconds, 0.7 milliwatt per bit; 4K device, 15-nanosecond access time, 0.2 milliwatt per bit; and 16K device, 25-nanosecond access time, 0.04 milliwatt per bit), n-channel MOS (NMOS), CMOS, or a combination of NMOS and CMOS. CMOS generally consumes much less power, about one quarter of that for NMOS. A 16K CMOS chip dissipates about 200 milliwatts. Figure 3 shows the average price per bit for 4K, 16K, 64K, and 256K SRAM, DRAM, and read only memories (ROM).

##### 2.2.1.1.3 Pseudostatic RAM

A new type of RAM has been introduced and the current chip capacity is 64K. It uses the small DRAM memory cell design and an on-chip control-refresh circuit to determine which cells are not in the read or write cycle and when they can be refreshed. It has the DRAM high cell density and acts as a SRAM to the system interface. However, the complicated control and refresh circuit reduces the overall chip capacity, reliability, and yield. The small gain in chip capacity makes it very difficult to compete with the true SRAM.

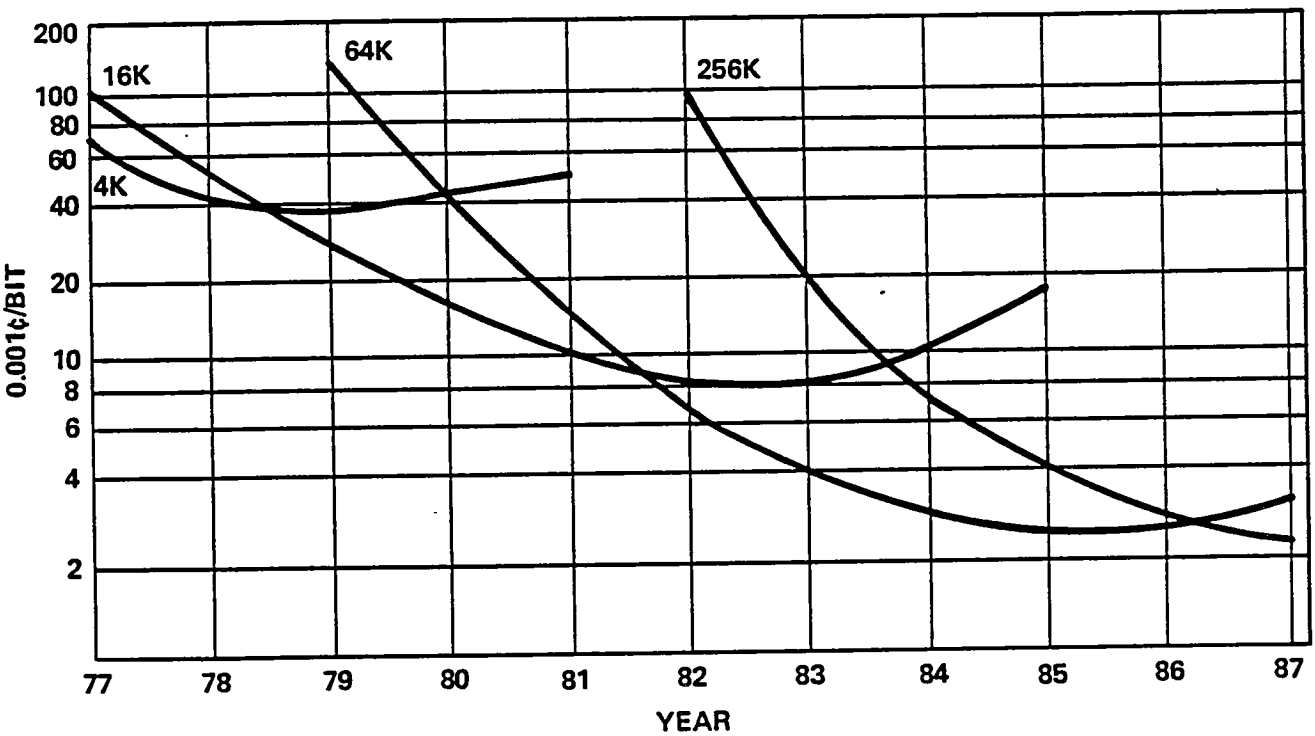



FIGURE 2. PRICE PER BIT VERSUS YEAR FOR VARIOUS DENSITY DRAM

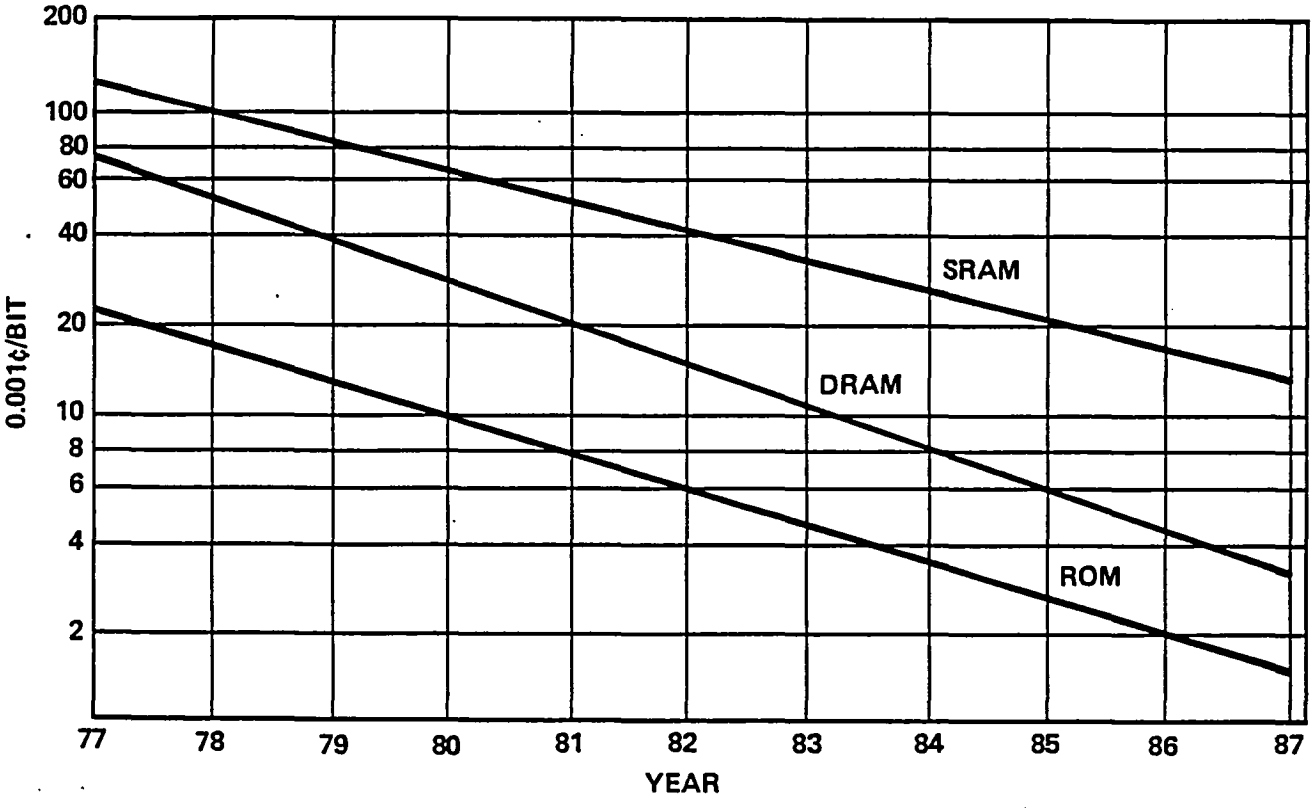



FIGURE 3. AVERAGE PRICE PER BIT VERSUS YEAR FOR SRAM, DRAM, AND ROM

#### 2.2.1.2 Nonvolatile Memory

The read and write of a nonvolatile semiconductor memory are usually based on different principles, use different processes, and operate at different speeds. The nonvolatility or data retention depends strongly on the write process and the principle on which it is based. The data retention period can be permanent or for several years. Some of the nonvolatile semiconductor memories are more appropriately classified as conditional nonvolatile memories.

##### 2.2.1.2.1 Read-Only Memory

Data are permanently programmed into the read-only memory device during manufacturing and cannot be altered by users. However, the memory cells are simple and small. 256K ROM are available now and 1M ROM are ready to be marketed. The access time is around 200 nanoseconds for 256K ROM and 350 nanoseconds up to 5 microseconds for the large 1M ROM. ROM always lead the nonvolatile industry in economy and density. Since new masks are needed for different memories, ROM are only cost effective when produced in quantity. They are selling at about 0.05¢ per bit, which is very close to that of DRAM but less than half that of the erasable ROM. ROM are also called mask read-only memories.

##### 2.2.1.2.2 Programmable ROM

Programmable ROM (PROM) are programmed by blowing minute fuses associated with the memory cells. The programming can be performed by users. However, it cannot be changed once programmed. For clarity, it is sometimes called fuse-programmable ROM. 64K PROM have been introduced but 256K chips are still several years away. PROM are available in bipolar (50-nanosecond access time) and CMOS (150-nanosecond access time) structures. Besides memories, PROM have also been used as fuse-programmable logic circuitry.

##### 2.2.1.2.3 Erasable PROM

The erase operation of an erasable PROM (EPROM) uses ultraviolet light, thus it is also known as ultraviolet erasable programmable read-only memory. The read-only memory name is misleading. The data can be rewritten but requires a clumsy and slow process compared with that of reading. It is suitable for read mostly applications. For erase, the chip has to be removed from a system and placed under an ultraviolet light for about one-half hour. An expensive package with an erasure window is required, and the entire memory must be erased. This was the first reprogrammable, nonvolatile memory. It provides its users an opportunity to alter the program and is very useful during the program development stage. EPROM is basically a MOS structure using two polysilicon electrodes (floating gate and control electrode) to control the charge present or absent on the floating gate, representing data bits one or zero. The memory cell, consisting of one transistor, is small (around 40 square micrometers). 256K chips are available today. EPROM require 12.5 to 20 volts to program, which is higher than the standard 5-volt operating voltage. It takes 50 milliseconds to program but the access time is about 200 nanoseconds.

##### 2.2.1.2.4 Electrically Erasable PROM

The structure and operating principle of the electrically erasable PROM (EEPROM) are similar to those of the EPROM: the floating gate is still used to store charges representing data bits. One important difference is that the charge is moved through the insulator to the gate by tunneling instead of by avalanche injection for the EPROM. To provide a high electric field for tunneling, the insulating layer thickness between the semiconductor and the gate has to be greatly reduced. Some manufacturers texture a thin polysilicon gate to create high fields at surface irregularities and thus ease the thin insulator requirement. EEPROM can be erased, programmed, and reprogrammed on a byte-by-byte basis with 5 volts. This provides versatility and in-circuit operation convenience. The programming takes about 10 milliseconds but reading requires only 100 to 200 nanoseconds. The memory has a $10^4$ charge-discharge cycle capability and a 10-year data retention time. SEEQ recently announced a $10^6$-cycle device based on their proprietary Q-cell design and oxynitride process. Faster write times can be

achieved by sacrificing the data retention time. For example, a 1-millisecond write time may be traded for 1 month retention time. A write time as short as 100 microseconds has been demonstrated. Since this technology is new, only 16K and 64K chips are being introduced. The performance and reliability need further study. For large quantities, SEEQ is selling 16K chips at $6 a piece, that is only 0.04¢ per bit. For small quantities, the price is estimated to be three times higher.

2.2.1.2.5 Nonvolatile RAM

The nonvolatile RAM (NVRAM) is a hybrid of the static RAM and EEPROM. It behaves as a static RAM to a user. However, the data are protected by the nonvolatile EEPROM during a power failure. This new memory version has the high-speed read and write of a static RAM and the nonvolatility of an EEPROM. Therefore, NVRAM are more suited for applications requiring frequent memory data changes. Since the EEPROM are only operating during power failures, the EEPROM cycling endurance and data retention time requirement can be relaxed. It is one of the most versatile memories in terms of features and capabilities. The memory cell complexity and the newness of the EEPROM have kept the NVRAM at the 1K- to 4K-bit capacity and a high price of approximately 1.3¢ per bit for a 1K chip made by Xicor.

Tables 2 and 3 compare the memory cell dimension and chip capacity of various semiconductor memories.

TABLE 2. MEMORY CELL DIMENSION

| MEMORY | APPROXIMATE CELL DIMENSION (MICROMETER) |
|---|---|
| Mask Programmable ROM (ROM) | 5 |
| Ultraviolet Erasable PROM (EPROM) | 7 |
| Dynamic RAM (DRAM)<br>Pseudostatic RAM (Pseudo SRAM) | 8 |
| Electrically Erasable PROM (EEPROM) | 13 |
| Fuse-Programmable ROM (PROM) | 14 |
| Static RAM (SRAM) | 18 |
| Nonvolatile RAM (NVRAM) | 45<br>(potential size 23) |

TABLE 3. CHIP CAPACITY

| MEMORY | YEAR | | |
|---|---|---|---|
| | 1979 | 1983 | 1987 |
| ROM, EPROM, DRAM | 64K | 256K | 1M |
| Fuse PROM, SRAM, Pseudo SRAM | 16K | 64K | 256K |
| EEPROM | - | 16 to 64K | 256K |
| NVRAM | - | 1K to 4K | 16K |

2.2.1.2.6 Combination ROM and EEPROM

The combination ROM and EEPROM (CREEM) takes advantage of ROM high capacity and high speed and at the same time solves ROM lack of data alterability once manufactured. Motorola has combined 14 Kbytes of mask programmed ROM with 2 Kbytes of erasable EEPROM to produce its 128K, 16K x 8-bit, CREEM. This arrangement provides a means to substitute the memory contents of the ROM for that of the EEPROM.

2.2.1.2.7 Metal-Nitride-Oxide-Semiconductor and Silicon-Nitride-Oxide-Silicon Memories

The metal-nitride-oxide-semiconductor (MNOS) and silicon-nitride-oxide-silicon (SNOS) memory transistors are nonvolatile, have a medium to high density, consume low power, are semiconductor packaged, can be randomly read fast, and can be radiation hardened. However, the memories have a limited number of read-write cycles, a slow erase-write, and limited suppliers. The memories are suitable for secondary memories and read mostly applications where ability to alter data is critical but fast read-write cycles are not important.

2.2.1.2.8 Complementary Metal-Oxide-Semiconductor Memory with Battery

The pairing of complementary n-channel and p-channel transistors to form low power consumption circuitry was invented in 1962. Because of the advancement made in recent years on CMOS cell packaging density, operating speed, reliability, and cost, CMOS configuration was used in the SRAM. 64K CMOS SRAM with an access time of 50 to 80 nanoseconds, an active power of 100 to 200 milliwatts and a standby power of 15 to 50 nanowatts have been announced. The low power consumption enables the CMOS SRAM to combine with a battery to form a practical, pseudo-nonvolatile memory. It provides fast read and write like a SRAM but retains data without external power.

Mostek Corporation is selling samples of 16K-bit CMOS with two emergency batteries and control circuits for about $20. That is equivalent to 0.12¢ per bit. The battery shelf life is about 10 years with a temperature range of 0 to 70°C. The RAM access time is 200 nanoseconds, active power is 275 milliwatts, and standby power is 5.5 milliwatts.

Using the special configurations of CMOS-SOS (silicon-on-sapphire) or CMOS-SOI (silicon-on-insulator), latchup problems are minimized, packaging density is increased, and radiation hardness is improved. The improvements are due to the isolation of n- and p-channel transistors provided by the insulating property of the sapphire (aluminum oxide) and the insulator (silicon dioxide). RCA demonstrated a radiation-hardened 4K CMOS-SOS RAM that is total dose hardened to 100 Krads (Si), free from latchup under transient radiation of $10^{11}$ rads per second and immune to cosmic ray upset to $2 \times 10^{-9}$ errors per bit day. However, the SOI configuration under development will be cheaper and more tolerant to thermal stresses.

**2.2.2 Magnetic**

Magnetic material is a favorite for memory because of its nonvolatility, radiation hardness, data retentivity, and unlimited number of read and write cycles. Furthermore, all magnetic memories are electrically reprogrammable.

2.2.2.1 Magnetic Core

The first generation of core memories was developed in the early Fifties. It is a mature technology and has a large commercial base. The core memory is randomly accessed, thus has no latency time. However, it uses destructive readout, which is undesirable in some cases. The longevity of the core technology is mostly attributed to the unavailability of suitable nonvolatile semiconductor or optical memories with no moving parts. The core memory may face the challenge of emerging semiconductor, optical, and magnetic memories in the late Eighties.

The characteristics of the core memory have been improved through the years by using smaller and faster cores. At present, a 64K-word, 18 bits per word module with dimensions of 6 by 9 by 0.9 inches is used in AN/UYK-43

and AN/UYK-44 military computers. The core has an outside diameter of 0.013 inch and an inside diameter of 0.008 inch. Three wires are strung through each core to form a 3D organization. Two wires carry half-select drive currents to switch the core at which they intersect. The third wire carries the sense signal from the selected core to the sense amplifier. This core module has a 900-nanosecond cycle time, a 350-nanosecond read time, a temperature range of minus 55 to plus 85°C, and a cost of slightly less than 1¢ per bit. It consumes 50 watts under typical operating conditions, requires 65 watts maximum power and 15 watts on standby power. A 128K by 18 bits module with dimensions of 6 by 9 by 1.4 inches, using 0.009-inch outer diameter, 0.006-inch inner diameter cores will be available soon. This smaller core module has approximately the same speed and power rating. It costs about the same as the 0.013-inch core module. An even smaller core having a 0.006-inch outer diameter for better core memory characteristics is being developed.

2.2.2.2 Magnetic Film

Ever since the successful experiments performed in the early Fifties to induce a magnetic anisotropy in evaporated polycrystalline magnetic films, there has been much research to make the magnetic film a very viable memory element. The magnetic anisotropy of a film is the variation of its magnetic properties as a function of orientation relative to a reference axis. This induced anisotropy is important because it provides a preferred direction or easy axis for the magnetization. Thus, it permits the magnetic thin film to be magnetized in either of two opposite directions along the easy axis; these two remanent states correspond to the 0s and 1s in a binary system. Magnetic films can be made having a square hysteresis loop (which permits coincident current switching), a low magnetostriction or strain sensitivity (for insensitivity to shock and vibration), and a high Curie temperature of 600°C for 81 per cent nickel (Ni) - 19 per cent iron (Fe) (for a wide temperature operating range). Magnetic film elements can also be made small for high density, low driving power, and fast rotational switching. Memory elements exhibiting read access time less than 100 nanoseconds have been demonstrated. In addition, the memory elements and the associated wiring can be fabricated and tested in multi-element arrays rather than as single elements. Magnetic film memories can be made either in nondestructive readout or destructive readout modes.

Sperry has been the pioneer and played a leading role in magnetic thin film memory. Early research led to a planar magnetic thin film 4K-bit scratch pad memory for the UNIVAC 1107 computer in 1961. Since then, planar thin film memory systems have been developed for a wide variety of militarized computer systems, including the CP-642B, the CP-667 and the UNIVAC 1830 computer. Continuing research resulted in the development (in 1967) of UNIVAC Mated Film Memory system that was adapted for the CP-808, the ASW S-3A AN/AYK-10 (UNIVAC 1832), and the AN/UYK-7 computers. The mated film element consists of two layers of magnetic film separated by a thin, narrow, insulated sense-digit line. Since the sense-digit line is narrower than the magnetic layers, the two magnetic layers can still be magnetically coupled to each other through the thin insulating layer. Storage of information is done in the same way as for a planar element, magnetization pointing in either of two opposite directions along the easy axis. The mated-film structure has a closed magnetic flux path. It minimized the at-rest demagnetizing field. It thus permits use of thicker film elements with corresponding larger output signal. It also reduces magnetization dispersion, lowers digit drive, and increases the threshold for magnetic creep and element imperfection for improved operating characteristics. The AN/UYK-7 double density mated film memory has a capacity of 32K words of 32 bits, a cycle time of 750 nanoseconds, consumes 250 watts, weighs 48 pounds, occupies 0.55 cubic foot, is randomly accessed, and is operated in a destructive readout mode.

A variety of magnetic film memories has been studied. In 1983 a novel, planar film, magnetic domain memory using chemically-deposited soft and hard exchange-coupled thin films was reported by Battarel of France. Localized magneto-static fields are created by a hard magnetic film deposited directly on the soft film. This structure permits the storage of very small domains and control of the domain propagation when the shift conductors are current pulsed. A 104K bits per square centimeter density has been obtained. The absence of an external bias magnet and the possibility of integration make the planar film, magnetic domain memory technology very competitive with the bubble memory technology for moderate storage capacities. However, the memory is accessed by block and the cycle time is of the order of 1 microsecond.

2.2.2.3 Plated Wire

The plated wire (cylindrical film) memory element is made of a beryllium–copper wire 0.005 inch in diameter electroplated with approximately 8000 angstroms (Å = $10^{-10}$m) thick layer of a non–magnetostrictive alloy of nickel–iron. A current in the wire during the plating process aligns the magnetic material to establish a magnetic preferred or easy axis circumferentially around the wire. The magnetization is stable along the easy axis. Thus, any section of the wire can be magnetized either clockwise or counterclockwise, corresponding to data bits one or zero. A memory plane consists of parallel plated wires inserted in tunnels formed in a plastic plane encircled orthogonally by word lines. The plated wires provide not only the storage medium but they also serve as the sense and digit (bit) line. The result is an orthogonal matrix of memory elements with the storage areas consisting of those portions of the plated wires located at the crosspoints where the word lines intersect the plated wires. This results in a low bit density of approximately 1000 bits per square inch. Information is written into the memory elements by applying coincident word and digit currents to the appropriate word line and plated wire. Reading is done by applying a word current to the word line. The word current generates a magnetic field that rotates the magnetization out of the easy axis. This action produces a change of magnetic flux that causes a signal voltage in the sense line representing data bit one or data bit zero. If the magnetic field used for reading does not exceed a certain threshold, the magnetization returns to its original orientation along the easy axis, either clockwise or counterclockwise around the wire, after the read field is removed. This makes the memory readout a nondestructive process. Smaller 0.002–inch and 0.0025–inch plated wires have also been manufactured. The smaller wire not only provides higher bit density than 0.005–inch wire but it also requires less drive current, thus reducing power dissipation.

The plated wire memory element has magnetic flux lines that are closed within the magnetic material. The closed flux path offers significant advantages over the open path that are characteristic of single layer planar film memory elements. One advantage is the possibility of using thicker film for a larger signal because there is no at–rest demagnetizing field to consider. The other advantage is the reduction of the digit (bit) current because of the high permeability of the closed magnetic flux path.

Mass plated wire memory with storage capacities of 10 million bits can perform a memory cycle at 1 microsecond and mainframe memories with capacities of 0.5 million bits can operate at 500 nanoseconds.

Plated wire memory element research was initiated at Sperry in 1961. Since then Sperry has developed memories for UNIVAC 9000 series and 1110 general purpose computers, the Minuteman AN/UYK–11(V)7 weapon system computer, and Rome Air Development Center. The plated wire memory is more suitable for military and space applications because of its operating speeds, nonvolatility, nondestructive readout, good radiation hardness, and reliability. However, it is expensive because it does not have a good commercial base. Although the plated wires are batch fabricated, the preparation of beryllium–copper wire prior to plating, the control of coercivity and magnetostriction of the plated film, and the assembly of the memory plane are difficult and time consuming. At present, the plated wire suppliers are limited to only two or three in the computer industry.

2.2.2.4 Magnetic Bubble

A garnet film with a magnetically preferred or easy axis normal to the film plane will present a set of serpentine domain patterns alternating in magnetization polarity. If a bias field normal to the film plane is applied and gradually increased, the serpentine domains with magnetization in the same direction as the field will widen at the expense of the oppositely–directed domains. When the bias field reaches a critical value, the shrinking domains will contract into isolated cylindrical domains resembling small soap bubbles when viewed through a Faraday effect apparatus. The cylindrical domains are stable when the bias field is held constant.

The magnetic bubble memory concept was proposed by Bell Laboratories in the late Sixties. The bubbles are those cylindrical domains just described in a magnetic garnet film epitaxially grown on a non–magnetic single crystal gadolinium gallium garnet substrate. The data bits are represented by either the presence or absence of the bubbles or by the different magnetic structures encoded in domain walls around the bubbles. The bubbles

can be electronically generated, propagated, transferred, replicated, detected, and annihilated to form a serially-accessed memory. These essential functions can be performed using magnetic thin film features deposited on the garnet in conjunction with an in-plane rotating magnetic field. This method is called field access. The functions can also be accomplished by providing deposited conductors or apertured current sheets on the garnet film and using pulsed currents in a method called current access. The bubble memory has no moving parts, is nonvolatile and suitable for applications in harsh environments.

A new version of bubble memory called Bloch line memory was proposed by Konishi of Japan in 1983. The data bits are represented by vertical Bloch line pairs, of the same sign, in the stripe domain walls in garnet films. Since the dimension of the vertical Bloch line pair and the stripe domain width are small, the memory cell size is small. It has been estimated that the Bloch line concept could lead to a bit density 30 to 100 times greater than that of the present bubble memory devices and a density of 1 billion bits per square centimeter.

The writing is done either directly, by applying fields to inject vertical Bloch line pairs into the stripe domain, or indirectly, by first generating the bubbles, then converting the presence or absence of bubbles to the presence or absence of vertical Bloch line pairs in a nearby stripe domain. Reading is done in reverse. The vertical Bloch line pair at the stripe domain end is converted to a bubble by applying a chopping, pulsed bias field. The bubble can then be detected by the conventional method. Propagation of vertical Bloch line pairs is done by applying successive pulsed bias fields and using the resulting gyrotropic forces induced by wall motion. Propagation does not require any small, deposited features as in conventional bubble devices, but potential wells along the data track may be necessary to better define the vertical Bloch line pair position and improve the propagation stability.

The essential memory function such as data write, read, and propagate have been demonstrated. However, in view of the complexity of the Bloch line control, especially during the vertical Bloch line pair propagation, this memory is not expected to be practical for quite some time.

2.2.2.5 Cross-tie Random Access Memory

Cross-tie random access memory (CRAM) is a magnetic thin film memory in which information is stored in structures within domain walls rather than in the domains themselves. It was discovered in the late Sixties that the very small size cross-tie structure (approximately 20 micrometers long and 1 micrometer wide) in the domain wall can be generated or erased by manipulating magnetic fields. Both the presence and absence of cross-tie states are stable when magnetic fields are removed. Hence, they can be used to represent data bits one and zero. The memory elements are made of polycrystalline nickel-iron films fabricated by vapor deposition or sputtering on glass, silicon, or other substrates. The cross-tie memory is a developing technology that has already reached the laboratory demonstration stage. The essential functions such as data writing in 20 nanoseconds and data reading in 270 nanoseconds have been demonstrated using a 16-bit memory array and a partially populated 8K memory array. Present efforts are directed toward design, fabrication, and evaluation of a fully populated 8K memory array to form the basis for a 16K memory chip. In its final form, CRAM will be externally indistinguishable from a static semiconductor RAM except for the fact that the data are nonvolatile. No refresh is required. The CRAM has no permanent bias magnets or moving parts. It can, therefore, be integrated using standard semiconductor processing procedures. It operates over the full military temperature range of minus 55 to plus 125°C, is radiation hard, and has a non-destructive readout. Write cycle time will be under 100 nanoseconds. Read cycle time will be under 500 nanoseconds.

A 16K by 1 CRAM will be the first chip to be fabricated by Sperry. The initial application is as a core module replacement for the AN/UYK-43 and -44 computers where one or two printed circuit cards filled with 16K CRAM chips can be configured in 64K by 18 or 128K by 18 organizations. The future CRAM chips should have a write cycle time of 20 to 50 nanoseconds and a read cycle time of 100 to 200 nanoseconds. When this goal is reached, CRAM will be able to replace semiconductor RAM in many applications in which nonvolatility is desired.

### 2.2.3 Other Memories

In addition to the various types of memories described, there are many other types being proposed, investigated, developed, manufactured, and marketed. Examples are electron beam addressable memory, magnetic domain tip propagation memory, ferroelectric memory, sonic film memory, woven plated-wire memory, optical memory, charge-coupled device memory, gallium-arsenide memory, Josephson junction memory, and Ovonic memory. Each has its own merits and difficulties. As new materials and new processing techniques upgrade the existing memories and new memory devices with better or different characteristics are introduced, some of the memories (including those described) will succeed and some will fade away. Five arbitrarily selected memories are described.

#### 2.2.3.1 Optical Memory

The data bit capacity (approximately $10^9$ bits) that can be achieved with no moving parts using either bit-by-bit or holographic page format is too small to be used for mass storage. The lack of a suitable page composer, a high resolution and fast light deflector, and a sensitive, high resolution, reusable recording medium also hamper further development work.

A $10^{15}$-bit, 1-nanosecond access, read, or write, 3-dimensional, random accessed, volatile (data must be refreshed at least once every 5 minutes), photon echo memory recently proposed by the Advanced Technology Laboratories of Vienna, Virginia, will encounter similar or more severe challenges.

#### 2.2.3.2 Charge-Coupled Device Memory

Data bits represented by charge packets are placed in specific storage elements created by designing potential wells in a semiconductor. These charge packets can be shifted from one storage element to an adjacent one by alternating the potential wells electrically. The charge-coupled device (CCD) memory is hence basically a shift register and is block-access oriented. Since each charge package may be of different size, it can be used as an analog shift register. It is a dynamic memory that requires periodic refreshing and is volatile. Although the data rate can be as fast as 10 MHz, its access time is long, (several milliseconds) depending on its capacity and organization. 64K and 256K CCD memories have been fabricated but are not competitive with the fast read and write DRAM. However, CCD are still widely used as image sensing and analog signal processing devices.

#### 2.2.3.3 Gallium Arsenide (GaAs) Memory

The high electron mobility and the semi-insulating characteristic of GaAs enable the fabrication of GaAs majority carrier devices to offer high speed and radiation tolerant integrated circuits. Advances in development are expected to achieve low power dissipation on the order of several microwatts per bit, access time on the order of several nanoseconds, and read-write cycle times on the order of tens of nanoseconds, radiation tolerance of $10^7$ to $10^8$ rads (Si), and operating temperatures of minus 200 to plus 200°C. At present, only small capacity (256 bits and 1K bits) static RAM have been demonstrated. No yield and cost data are available. The challenge is to increase yield via improvement of GaAs substrate quality and processing techniques.

#### 2.2.3.4 Josephson Junction Memory

Extremely high-speed, low-power memories have been demonstrated using Josephson Junctions (tunnel junctions between superconductors). State of the art is a fully decoded 4K-bit memory chip with 500-picosecond access time and 100-microwatt power consumption. Because the data are represented as supercurrents flowing in rings, the data are retained when power is off. Disadvantages are the need for low temperatures (below 10 degrees kelvin) and fabrication difficulties. However, low temperature permits use of superconductive strip lines and ground planes, and reduces electrical noise. Bit selections for write and read (both destructive and non-destructive readouts) are made with coincident current techniques similar to the core memory. IBM has been a major developer of this technology since the Sixties.

### 2.2.3.5 Ovonic Memory

Each memory cell consists of an Ovonic (or Ovshinsky) amorphous semiconductor device and an isolating diode in series on a silicon substrate. Many such cells are arranged in an array with each cell addressable by an x–y grid. The cell behaves like a nonvolatile bistable resistor with an on–to–off resistance ratio of about $10^3$:1. The high and low–resistance states are used to represent data bits one and zero. The series diodes are required to prevent any undesirable resistance shunting effect presented by the adjacent Ovonic devices.

Changing the memory cell from a high–resistance (disordered, glassy, or amorphous) state to a low–resistance (ordered or crystalline) state and vice versa (that is, writing), is done by applying a pulse of a certain voltage, current, and duration. The cell can then be interrogated, or read, without changing its state by applying a constant current and measuring the voltage to determine whether the Ovonic device is in its high or low resistance state.

Advantages of this type memory are its nonvolatility, electrical alterability, and fast nondestructive readout. For a 256–bit memory array, a 65–nanosecond read time has been demonstrated using 5 volts and 2.5 milliamperes. The disadvantages are the nontypically high voltage (25 volts), large current (200 milliamperes), and long pulse times (10 milliseconds) required for writing data in the memory. It is more suitable for use as a read–mostly memory. The repeatability of the Ovonic device has been reported by Energy Conversion Devices to be very good. Only a small change in characteristics was observed after a lifetime test of $10^{12}$ cycles.

# SECTION 3

# REQUIREMENT AND SELECTION

## 3.1 REQUIREMENT

The primary consideration of memory devices for commercial uses is cost. The users are generally satisfied as long as the devices have reasonable speed and adequate reliability. The memory devices' tolerance to temperature, vibration, humidity, radiation, and nonvolatility are seldom emphasized or even required. On the other hand, the characteristics important to military and space applications are many:

- High reliability
- Availability
- Nonvolatility
- Maintainability
- Security
- Operation in severe environment (temperature, humidity, shock and vibration, and electromagnetic fields)
- Small physical size
- Low weight
- Low power
- Radiation hardness
- Single event upset tolerance

Military and space memory research and development are directed toward achieving these characteristics. Other goals are to eventually improve the life cycle cost, programmability, speed, volume, and power consumption of the present memory devices.

## 3.2 SELECTION

As stated in Section 1, many types of memories and technologies have been proposed and investigated. However, when the desired military and space application characteristics are considered there are only a few suitable candidates. As shown in Figure 1, a spectrum of memories extending from the slow, serially accessed tapes to the fast, semiconductor and magnetic RAM is presented. In the selection of memory devices for military and space applications, the tape and disk are not desirable, mainly because of their moving parts. The CCD, DRAM, and SRAM are also not desirable because of their volatility. Finally, core and plated wire are more desirable although still not totally satisfactory because of their high cost and bulky, individually fabricated memory elements. Only five memories (CMOS with battery, EEPROM, MNOS, bubble, and cross-tie) remain as desirable selections as shown in Figure 4.

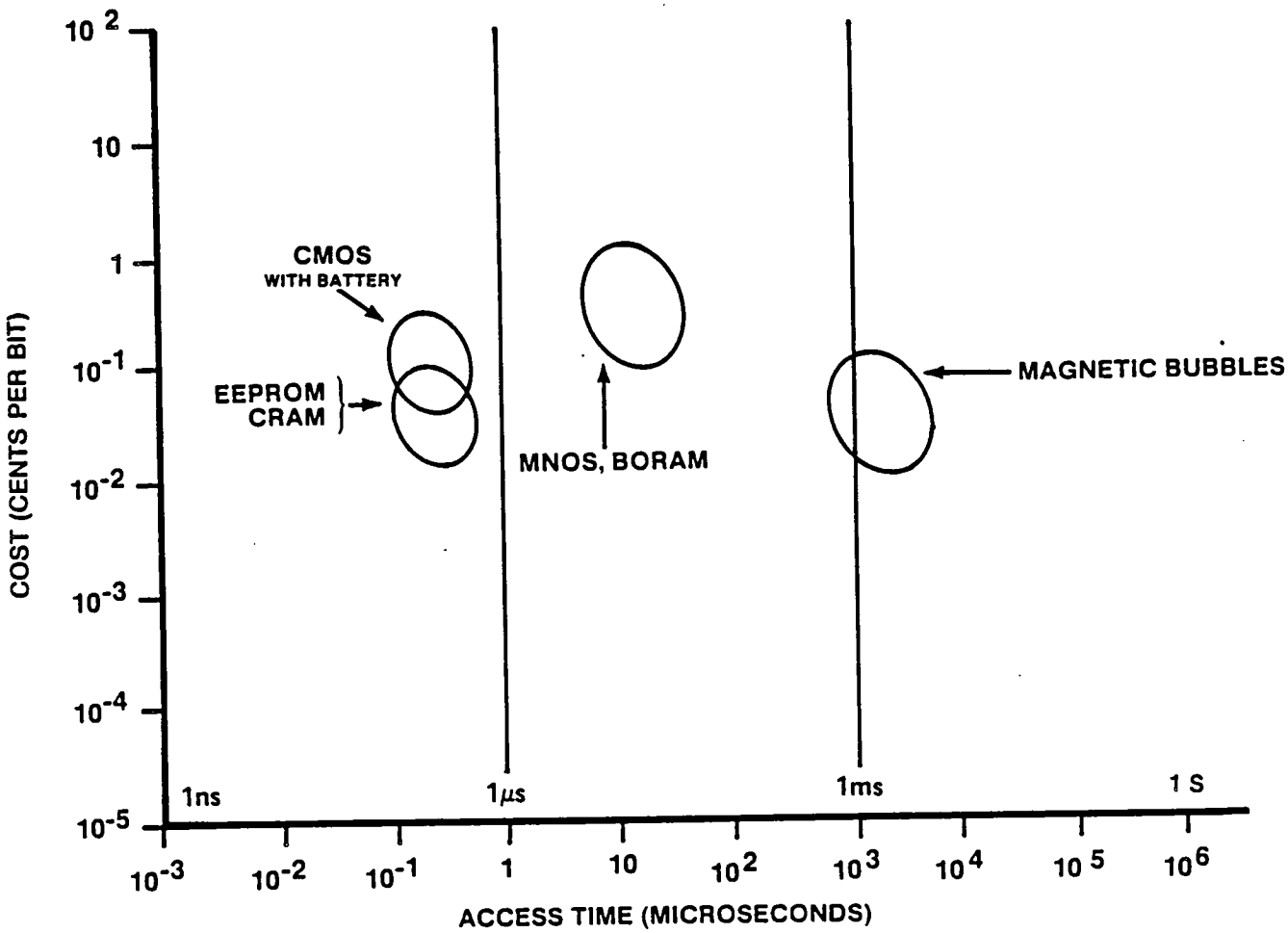



FIGURE 4. MEMORY TECHNOLOGY SELECTION

# SECTION 4

# DISCUSSION

## 4.1 COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR MEMORY WITH BATTERY

CMOS with battery is a pseudo nonvolatile memory with fast read and write times that requires low operating and standby power. Figure 5 shows several CMOS configurations. To isolate adjacent transistors, CMOS can be fabricated on silicon islands grown on top of the insulating sapphire substrates to form a silicon-on-sapphire configuration or on top of a silicon dioxide insulating layer to form a silicon-on-insulator configuration for better density and radiation hardness.

Mostek Corporation offers 16K samples with two self-contained batteries for $20. They have an access-read or -write cycle time of 150 to 250 nanoseconds, an active power of 275 milliwatts, a standby power of 5.5 milliwatts, and require only plus 5 volts. No additional support circuitry is needed to interface to outside systems. These samples are candidates for applications where batteries are allowed. A block diagram of this self-contained solution to RAM volatility is shown in Figure 6. When the power supply voltage is above 4.75 volts the static RAM is fully operational. When the voltage is between 4.75 and 4.5 volts the SRAM automatically write-protects itself. Once the voltage is below 4.5 volts, all inputs to the RAM are disabled. As the voltage falls below 3 volts the power switching circuit connects to one of the better lithium cells. Nevertheless, problems associated with batteries should be considered, for example: the electrical and mechanical interconnection between the batteries and the silicon chips, sensitivity of the batteries to pressure, space, weight, limited life, and lack of experimental data for aerospace and military environment.

Compared with EEPROM, the battery-backed SRAM made of CMOS cells has broader application and is simpler to use if batteries can be tolerated.

## 4.2 ELECTRICALLY ERASABLE PROGRAMMABLE READ-ONLY MEMORY

EEPROM evolved from the electrically programmable read-only memory (EPROM). Both devices operate on a similar principle and have a similar structure as shown in Figure 7. The floating gate is for charge storage: when there are electrons on the floating gate, the channel between the source and drain of the transistor does not conduct, representing a data bit zero. When there is no electron, the channel conducts and a data bit one is represented. To charge a gate, a voltage is applied to the selection gate to control the charging process. The main differences between EPROM and EEPROM is that the EPROM uses avalanche injection while the EEPROM uses the Fowler-Nordheim tunneling mechanism. Since the tunneling occurs at a field strength of $10^7$ volts per centimeter ($10^6$ volts per centimeter if surface irregularities exist), the tunnel oxide thickness is reduced to the range of 100 to 200 Å to lower the required tunneling voltage to an acceptable level of 20 volts. Some designers use a textured gate surface to locally enhance the field strength for achieving tunneling at a lower voltage with a thicker tunnel oxide layer. An oxide layer of approximately 800 Å combined with a textured surface has been used in EEPROM. The thick oxides are easier to fabricate and also lead to longer data retention due to the lower leakage current during readout. Furthermore, EPROM must be erased using an ultraviolet light after the memory package is removed from the system. The EEPROM erase can be done in the system, and requires only a 5-volt power supply. The feature of electrical erase and write on a selected bit, a byte, or block basis is essential to many applications. The EEPROM provides data alteration capability not only in the system, on-the-spot, but also at a distant location via control-communication lines. It offers a random access read time of 200 to 300 nanoseconds and can be read an indefinite number of times. However, the EEPROM is not without limitations. It usually requires 10 milliseconds to erase-write (program), thus causing processor delay without timing and control circuitry. The number of times data can be written (charge can be stored in the floating gate) is limited, typically $10^4$ cycles. SEEQ has announced their 16K 5516A EEPROM capable of $10^6$ cycles. The device is based on their proprietary Q-cell design and oxynitride process. The data retention time (nonvolatility) is also limited to a 10-year period. Xicor sells both the 16K and 64K chips for about 0.15¢ per bit. EEPROM are also available for a military temperature range of minus 55 to plus 125°C.

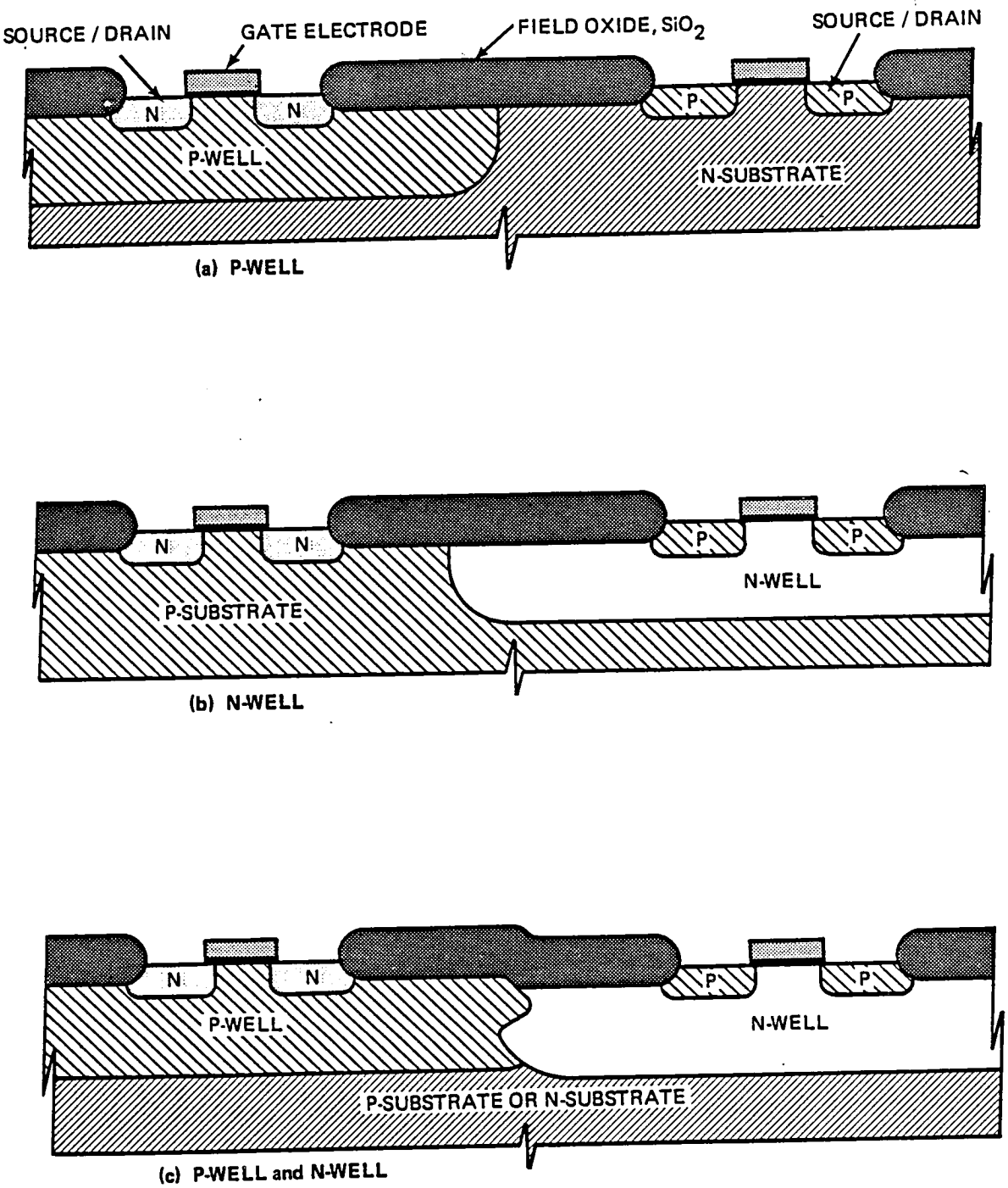



FIGURE 5. CMOS CONFIGURATIONS

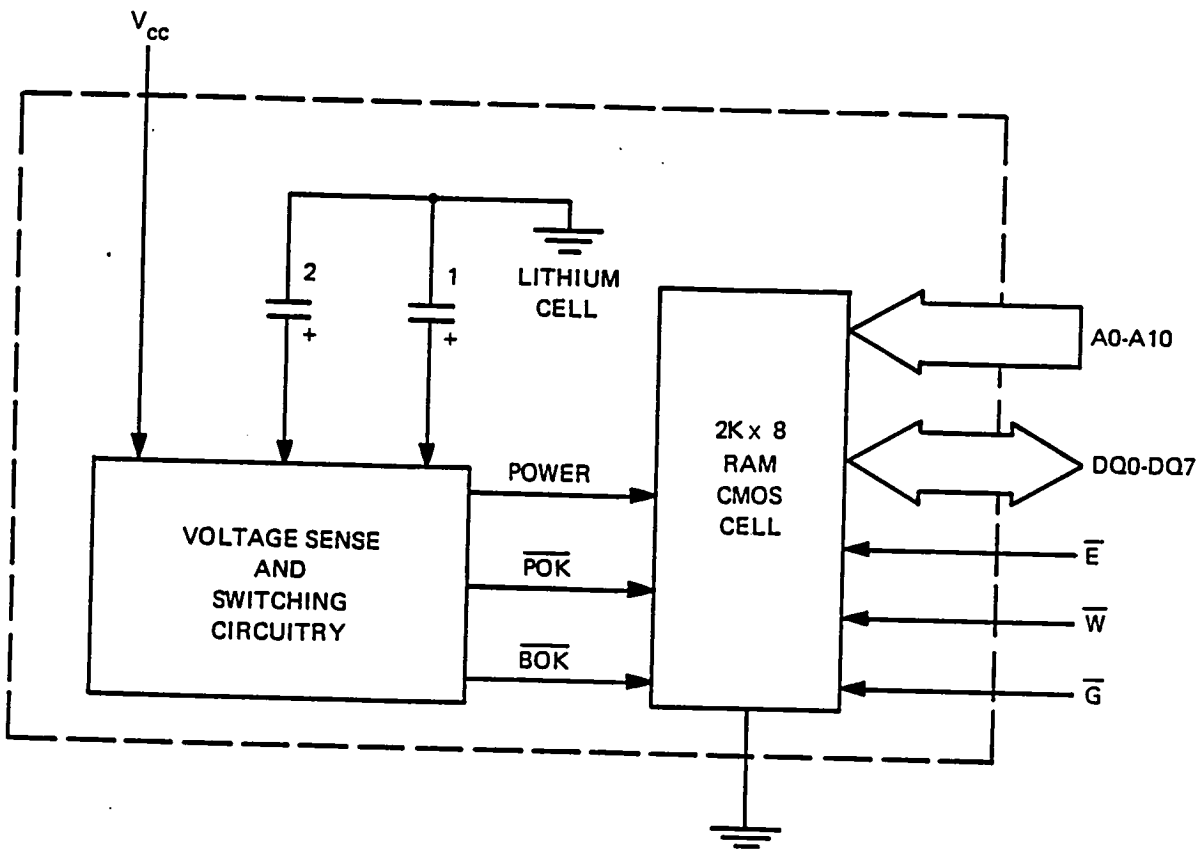



FIGURE 6. SELF-CONTAINED CMOS CIRCUIT

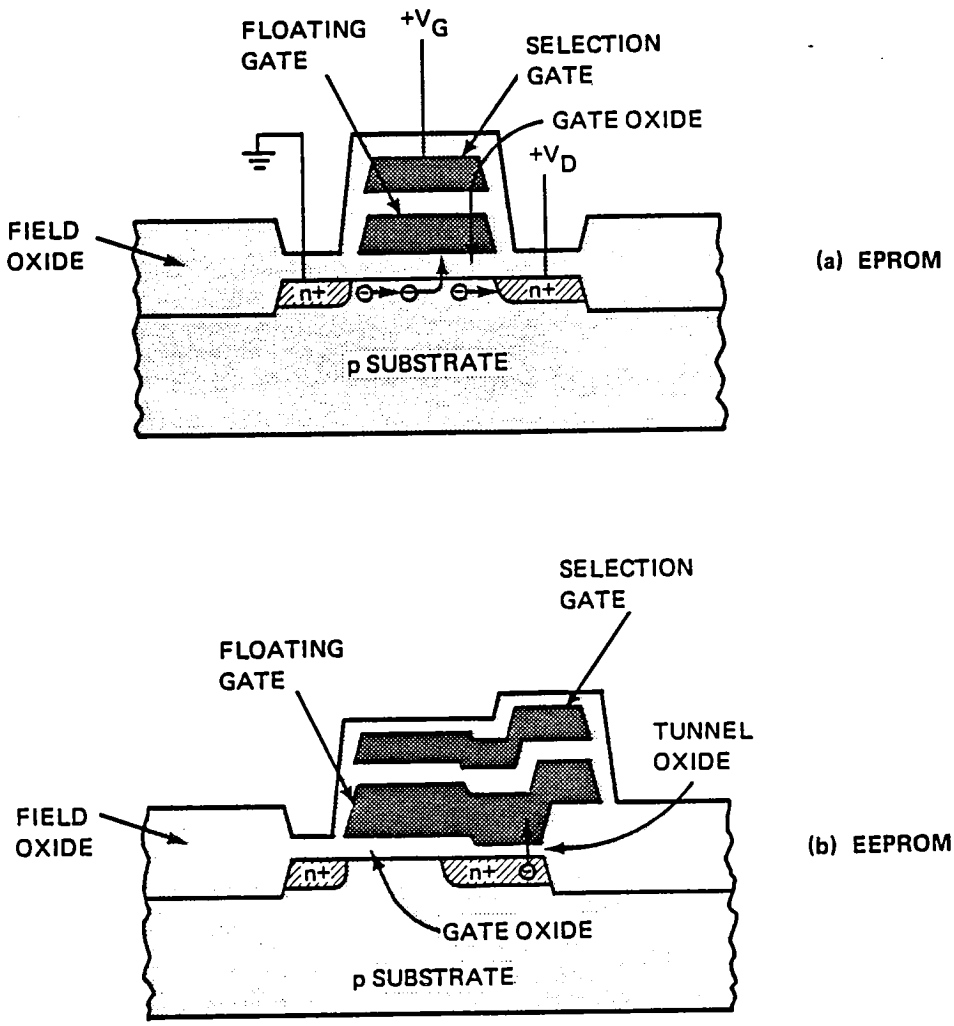



FIGURE 7. EPROM AND EEPROM CELL STRUCTURES

Overall the EEPROM is a very attractive, nonvolatile memory offering 5-volt operation; an electrical erase in place, in the system; various bit, byte, or block programming options; and a random access read time of 200 nanoseconds. These characteristics make it a good candidate for many applications. However, the system using EEPROM should be able to tolerate the slow 10-millisecond write time, the limited $10^4$ write cycles, and the 10-year data retention time. Due to its slow write time and fast read time, EEPROM is most suitable for applications calling for infrequent memory writes.

Now is an appropriate time to compare the EEPROM with the battery-backed CMOS RAM. What are the advantages of EEPROM compared to the CMOS RAM? The read and write speed, number of write cycles, power consumption, ease of use, and the cost of EEPROM are either comparable or inferior to those of the CMOS RAM. The only distinct advantage of EEPROM is nonvolatility that doesn't rely on batteries, with their associated problems. EEPROM are suitable for small capacity memories and in remote or hazardous areas where battery replacement or inspections are inconvenient.

### 4.3 METAL-NITRIDE-OXIDE-SEMICONDUCTOR AND SILICON-NITRIDE-OXIDE-SILICON MEMORIES

The metal-nitride-oxide-semiconductor (MNOS) memory transistor is the first electrically alterable nonvolatile semiconductor memory. It is known as MNOS EAROM (electrically alterable read-only memory), MNOS EEPROM, or nonvolatile MNOS RAM. Clarification of the MNOS structure is important to avoid confusion with the floating gate electrically erasable memories. A p-channel MNOS configuration is shown in Figure 8. It uses the charge carrier traps in the nitride near the nitride-oxide interface to store charge that represents data bits. The MNOS configuration has been studied since the Sixties and is a mature memory technology. It consumes low power; has a medium storage density, a wide operating temperature range, and a fast read; and is electrically alterable and nonvolatile. However, it has a limited number of slow erase-write cycles and limited data retention time. Because of the slow erase-write cycle, MNOS memories sometimes are organized in a block oriented manner to increase the effective data erase-write rate. Sperry's 14-lead flatpak, 8K MNOS BORAM, is organized in 256 blocks by 32 bits offering high performance in a block oriented mode. This memory is nonvolatile, can be operated over the minus 55 to plus 125°C temperature range, has a block write time of 1 millisecond, a block access time of 15 microseconds, a data rate of 2 megahertz, and a price of 0.4¢ per bit. It uses approximately 500 milliwatts operating power or 0.5 milliwatt standby. It features a $10^{11}$-cycle nondestructive read, a $10^8$-cycle write, and a $10^4$-hour data retention time. It is most suitable for read applications where ability to alter nonvolatile data is critical but a fast read-write is not required.

A modified version using polysilicon gate and n-channel has been developed and is called silicon-nitride-oxide-silicon (SNOS) configuration. It has a shorter channel length combining with the high mobility of the n-type silicon (1700 centimeters square per volt-second), resulting in a higher density and a faster speed. The polysilicon gate also provides more flexibility in fabrication processes. Several 16K and 64K chips with different structures, materials, and number of gates have recently been reported. The reported data varies for different device designs, in operating temperature, retention, and density. Hitachi's 5-volt only 8K x 8 SNOS memory is packaged in plastic with 28 pins. It has a 200-nanosecond access time, takes 60 milliamperes typical and 18 milliamperes standby, requires 1 millisecond to program a byte and 10 milliseconds to erase a byte or chip, retains data for 10 years at 85°C (1 year at 300°C), and has a capability of $10^4$ erase-write cycles.

Both the MNOS and SNOS devices can be radiation hardened at the expense of speed, density, and cost. It should be more immune to the radiation induced charge loss than the floating gate devices because charges are stored in the dielectric and the charge quantity is larger.

A radiation-hardened 16K-bit (2K x 8) silicon gate CMOS-NMNOS electrically alterable ROM has been designed, fabricated, and evaluated at the Sandia National Laboratories. Table 4 lists the characteristics.

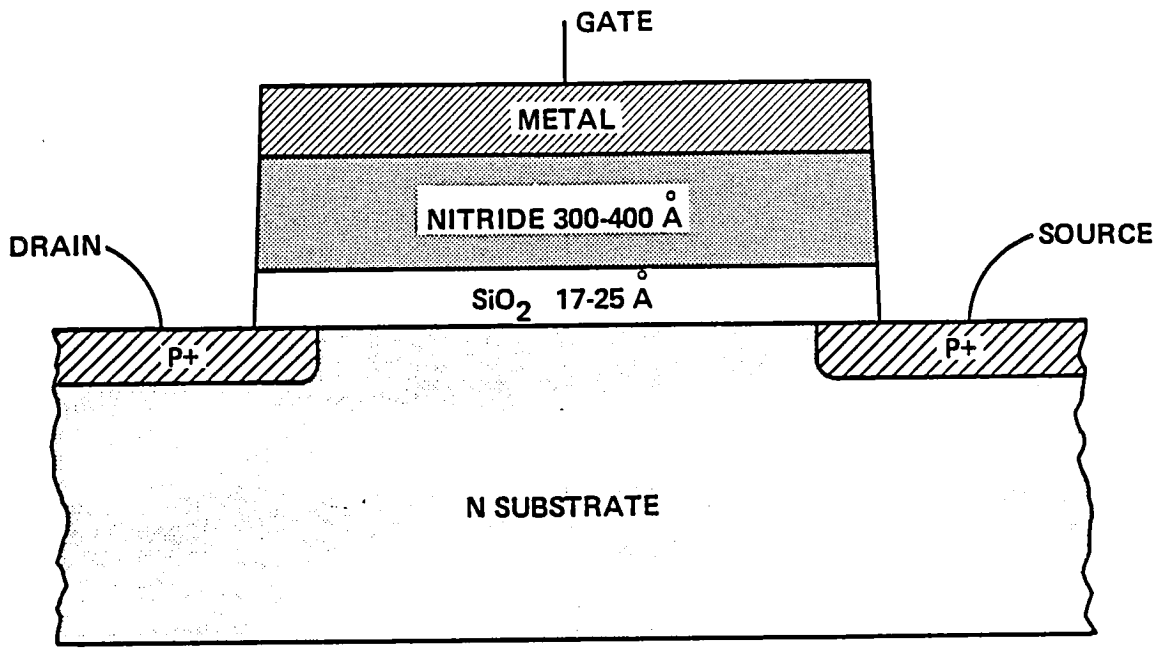



FIGURE 8. MNOS MEMORY TRANSISTOR

TABLE 4. SANDIA RADIATION-HARDENED 16K-BIT CMOS-NMNOS

| FEATURE | CHARACTERISTIC |
|---|---|
| Technology | Silicon-gate NMNOS memory array<br>Silicon-gate P-well CMOS control logic |
| Clear time | 100 milliseconds, block (16K-bits) or page (16 words) clear |
| Write time | 10 milliseconds |
| Endurance | 10,000 cycles |
| Read access | Less than 300 nanoseconds |
| Retention | 10 years (no read disturb) |
| DC voltages | $V_{DD}$ = 4.5 to 12 volts, $V_W$ = 18 volts (±10%) |
| Standby power | Less than 100 microwatts |
| Temperature | −55 to +125°C |
| Interface | SA3000 (8085) bus compatible |

The memory cell size is 28 micrometers by 28 micrometers. The increase in size is primarily due to the P + guardband required to isolate the cells. It is fully functional at $10^6$ rads (Si) total gamma dose. Logic upset occurred at 5 x $10^8$ rads (Si) per second but no dose-rate-induced data loss or latchup was observed up to 5 x $10^{11}$ rads (Si) per second for a 20-nanosecond half-pulse width. The 100-millisecond clear time and 10-millisecond write time are for a 10-year retention after $10^4$ clear-write cycles, post radiation, and at 125°C. Short clear and write times may be used for shorter retention times and less severe environment.

At Sperry, an experimental metal-gate, p-channel, radiation hardened chip of 256 bits withstanding a total gamma dose of 3 x $10^5$ rads (Si), a gamma dose rate of 2 x $10^{12}$ rads (Si) per second for a 40-nanosecond half-pulse width, and a neutron irradiation of 3 x $10^{14}$ neutrons per square centimeter was demonstrated in 1977. It had a retention of only 1 day but a faster cycle of 2 microseconds and a read access time of 1 microsecond.

In general, the capacity of the radiation hardened chips is usually two generations behind that of commercial ones.

Summarizing the three semiconductor memory discussions on CMOS with battery, EEPROM, and MNOS or SNOS, Tables 5 and 6, containing the nonvolatile semiconductor memory cell evaluation criteria and structure-technology options, are presented.

TABLE 5. EVALUATION CRITERIA

| | |
|---|---|
| • Retention | • Endurance |
| • Read disturb | • Program–erase disturb |
| • Read current | • Program–erase speed |
| • 5–Volt operation | • Program–erase voltage and current |
| • Density | • Scalability |
| • Complexity | • Compatibility |

TABLE 6. STRUCTURE AND TECHNOLOGY OPTIONS

| FEATURE | CANDIDATE |
|---|---|
| Basic structure | Floating gate or MNOS |
| Transistors or cells | One, two, three, or four transistors |
| Cell selection | Select transistor or capacitor |
| Charge carriers | Electrons or holes |
| Transport mechanism | Tunneling or hot carrier injection |
| Transport medium | Oxide (O), Nitride (N), ON, NO, or ONO |
| Transport path | Top dielectric only, bottom dielectric only, or both |
| Injection electrode | silicon, polysilicon, textured poly, or silicon rich |

## 4.4 BUBBLE MEMORIES

### 4.4.1 General Description

Bubble memories use the property of magnetic garnets to support small regions of reverse magnetization as shown in Figure 9. Under certain conditions these regions, or domains, are nearly circular when viewed from the top of the garnet, and are referred to as bubble domains. A more general description of this region is a right circular cylindrical domain. Data stored in a memory device are coded in binary form by the presence or absence of bubble domains. The domains are caused to propagate under the influence of local magnetic fields (described later) to perform various memory functions.

Commercially available bubble memory devices are generally designed with a block replicate organization comprising major bubble propagation lines and minor bubble propagation loops as shown in Figure 10. The minor loops are the main storage area, and are shown in the central region of Figure 10. The major line skirts the ends of all the minor loops, and includes the input and output tracks to perform the data input and output functions. Functionally, the bubble memory is comprised of three sections: a storage area composed of minor loops, an input port composed of a bubble generator and a set of transfer–in gates, and an output port composed of a set of replicate or transfer–out gates and a magnetoresistive detector.

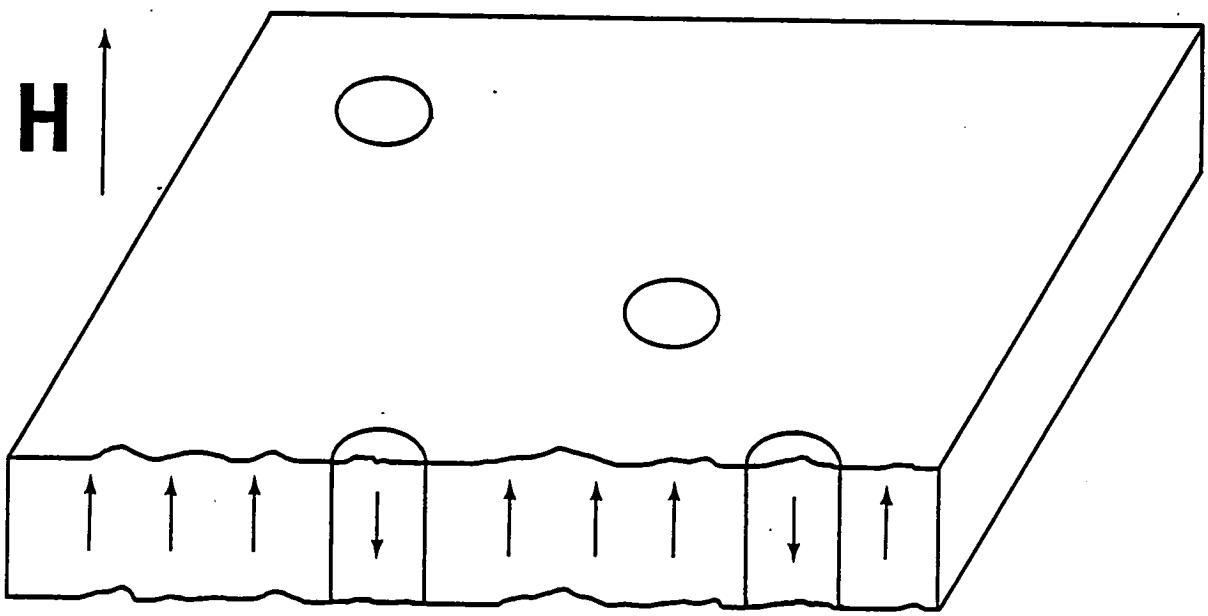



FIGURE 9. BUBBLE DOMAINS IN A GARNET SUBSTRATE STABILIZED WITH AN APPLIED MAGNETIC FIELD H

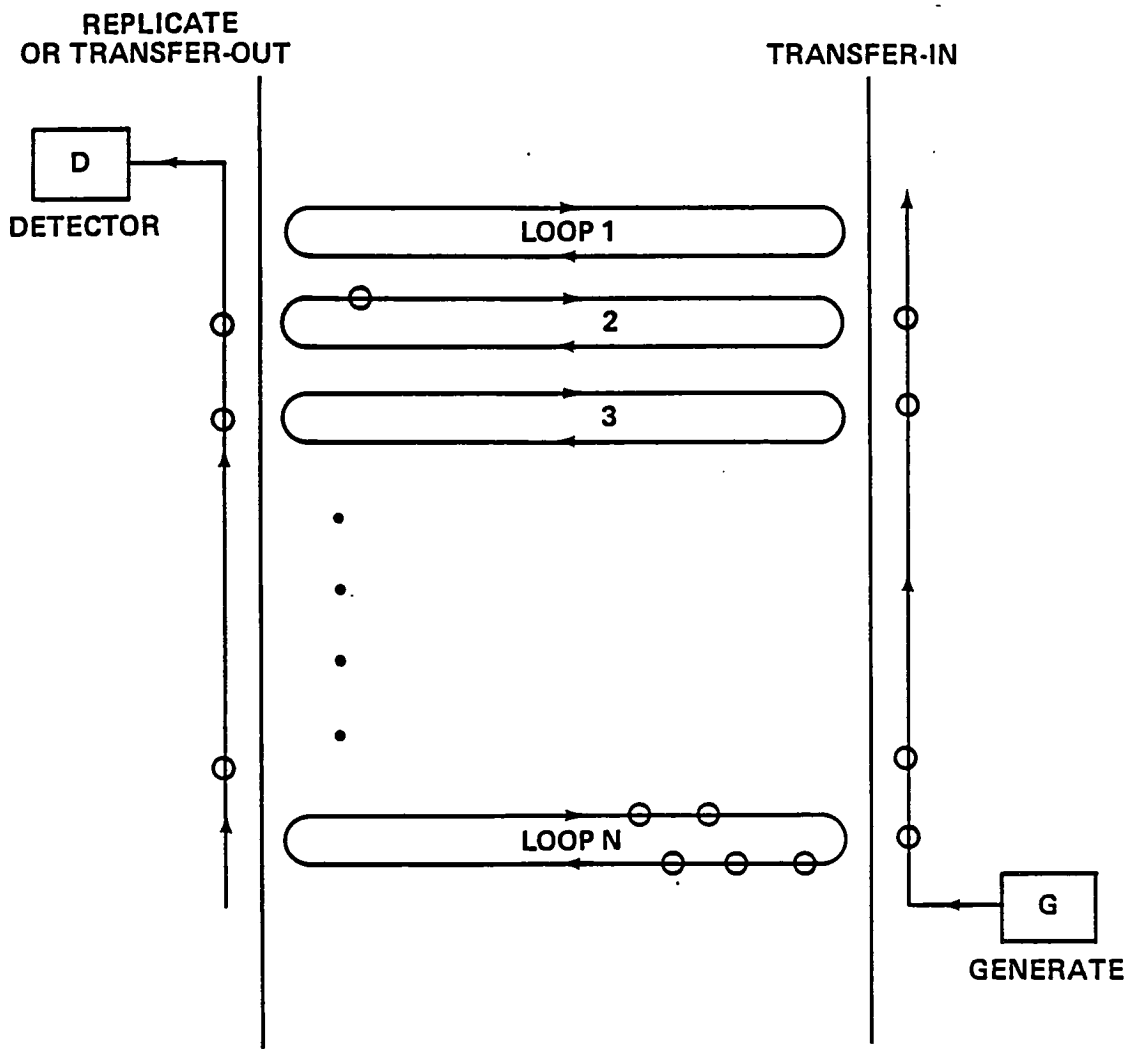



FIGURE 10. MAJOR LINE-MINOR LOOP ORGANIZATION

A major line–minor loop design is incorporated to reduce the average access time of a memory. A memory with $N^2$ bits and a bubble transit time of T for one propagation period has an average access time of NT with this design. For example, $N = 10^3$ bits and T = 10 microseconds (f = 100 KHz), and NT = 10 milliseconds. A simple shift register memory design has an average access time of $0.5N^2T$, which is much longer for large values of N. For the same example, the access time of $0.5N^2T$ will be 5 seconds instead of 10 milliseconds.

Inside the memory package, the bubble–supporting garnet substrate is located inside two orthogonal sets of wound coils that establish an electronically generated magnetic field that rotates in the plane of the bubble garnet. Propagation features of NiFe, which are defined on the garnet by photolithographic techniques, generate local magnetic fields normal to the garnet surface due to their interaction with the applied in–plane field. Bubbles are attracted to different portions of the propagation features as the in–plane field rotates, as depicted in Figure 11. All of the bubbles in the memory chip advance one position for each 360 degrees of rotation of the in–plane field. Circulation of the bubble domains around the device circuit loops into their proper positions allows read, write, transfer–in, and transfer–out or replicate functions to be performed.

Nonvolatility of the stored data is ensured by permanent magnets arranged so that their generated field is perpendicular to the surface of the bubble garnet substrate. This field satisfies the stability conditions required to support magnetic bubble domains. The permanent magnets are selected with a temperature coefficient of magnetization that matches the garnet material, thereby ensuring that the bubble diameter is nearly constant over an extended temperature range.

Bubble memories have the desirable properties of nonvolatile data storage, radiation hardness, wide operating temperature range, low cost, and moderate power dissipation. A typical 1 million–bit chip operates at a frequency of 100 KHz with an average access time of less than 12 milliseconds, weighs 30 grams, has a package size of 1.2 by 1.1 by 0.4 inches, operates over a 0 to 70°C temperature range, will retain data over a minus 40 to 100°C range without power, and consumes approximately 1 watt operating at 100 KHz.

Bubble memory packages containing 1 million–bits are presently available from a few suppliers for $200 in large quantities. One supplier quotes $99 for very large quantities for delivery late in 1984, and represents a cost of the memory of only 0.01¢ per bit. Memory packages containing 4 million–bits are presently under development (Intel 7114).

One million–bit memory chips having a minus 40 to plus 85°C temperature range are also available but at a higher price of approximately 0.05¢ per bit.

### 4.4.2 Future Developments

One of the basic limitations of the commercially available bubble memories is the inability to fabricate small propagation features. Asymmetric chevron features require a gap slightly smaller than the bubble diameter, and also have a pattern period whose length is many times the bubble diameter. Both of these factors limit the ultimate bubble density due to photolithographic constraints and cell size.

Charged wall, or contiguous disk, bubble devices are presently under development. This reduced photolithographic requirements for its propagation features. This allows a greater bit density to be established. Manipulation of bubbles is also done with a rotating in–plane magnetic field.

Another basic limitation of bubble memories is its low frequency of operation resulting in a slow data rate. This limitation is caused by the wound set of coils that generate a rotating magnetic field required for bubble propagation. Due to the inductance of the coils, as the frequency of operation increases, the required driving voltage rises rapidly, which is limited by the solid state drivers.

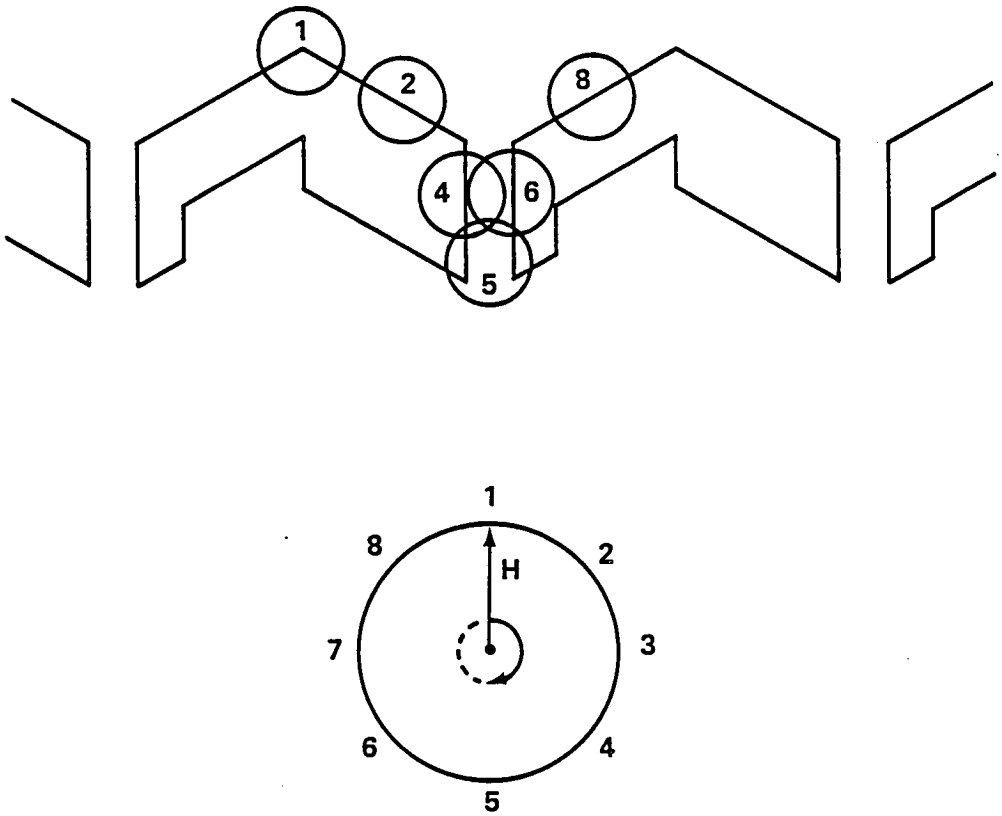



FIGURE 11. BUBBLE PROPAGATION WITH MAGNETIC ASYMMETRIC CHEVRONS UNDER THE INFLUENCE OF A ROTATING IN-PLANE MAGNETIC FIELD H

Memory designs have been proposed that use current-access techniques instead of the rotating field access concept. The coil sets to produce a rotating field are eliminated, and bubble propagation is caused by current carrying conductors placed on the garnet substrate. As a result, the frequency of operation of laboratory test devices increased to values exceeding 1 megahertz.

One of the current-access memory designs presently under development incorporates a self-structured bubble concept that uses the natural properties of bubble garnets for device design. Bubbles in storage are arranged in a lattice, which is the naturally occurring hexagonal pattern for closely spaced domains. Propagation is done with apertured dual conductor sheets, which do not have the gap bubble diameter problems associated with magnetic propagation features. A double layer garnet is used, one layer of fully populated bubbles acts as a carrier layer. A second layer, containing partially populated data bubbles, magnetically couples to the carrier bubbles. An increase in bubble density by a factor of 10 to realize a $10^7$-bit chip, and an increase in the operating frequency of at least a factor of 10 to realize a 1-MHz bit rate is feasible for the self-structured memory concept as compared with present commercial bubble memories.

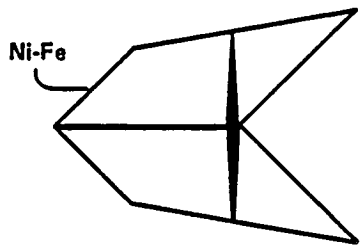
### 4.4.3 Summary

Bubble memory is a magnetic technology that is intrinsically radiation hardened and nonvolatile. It requires no battery back up and has an unlimited number of write-read cycles. Since it has no moving parts and is resistant to shock, heat, humidity, and dust, it is suited for robotics, oil drilling rigs, flight recorders, and many other industrial, military, and space applications operating in harsh environments. Its nonvolatility and portability enable the bubble memory to be used as a form of working storage in a portable computer. Bubble memories are more reliable, lighter, smaller, and faster than tape cassettes and flexible disks. However, the bubble memory is not without faults. It is more expensive, requires multiple voltage power supplies, consumes considerable power, has a long access time, is generally organized in block read and write mode, has a slow data rate, does not have a full military specification operating temperature range, needs support chips, and is difficult to interface. Since the bubble memory is fabricated on a magnetic garnet, the support circuitry cannot be integrated on the same chip. In addition, the memory chip package needs permanent magnets, two perpendicular field coils, and special magnetic shielding.

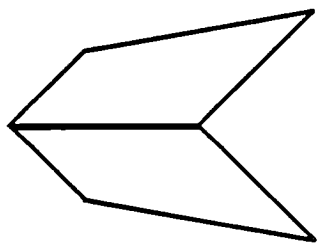
Nevertheless, bubble memories of 1 million-bit and 4 million-bit capacity are the most dense, batch fabricated, radiation hardened, and nonvolatile solid state memory now available. Bubble memories possess great radiation hardness in spite of the single crystal structure of the garnet. Bubble memories remain operational without failure after exposure to a neutron irradiation of $10^{15}$ neutrons per square centimeter, a total gamma dose of $5 \times 10^7$ rads (Si), and a gamma dose rate of $3 \times 10^{11}$ rads (Si) per second for a 30-nanosecond half-pulse width.

## 4.5 CROSS-TIE RANDOM ACCESS MEMORY

The cross-tie random access memory (CRAM) is a solid state, nondestructive readout, nonvolatile random access memory that uses the magnetic cross-tie structure in nickel-iron (NiFe) thin films as a memory element. The element is designed as shown in Figure 12 to allow the existence of either a cross tie or no cross tie depending on the history of the magnetic field. The presence of a cross tie is a one and its absence is a zero. The state of the bit is sensed by a magnetoresistive detector as shown in Figure 13, one of which is located at each memory cell. Magnetoresistance is the property of certain materials including NiFe for which different electrical resistance is displayed depending on the material's own state of magnetization. Based on this principle, the resistance is highest when a current (I) is parallel to the magnetization (M), lowest when the current is perpendicular to the magnetization. Hence, the voltage across the detector would be higher for the presence of a cross-tie as shown in Figure 13(a) because of the 45-degree angle between I and M and lower for no cross tie because of the 90-degree angle between I and M as shown in Figure 13 (b).




(a) CROSS TIE: ONE



(b) NO CROSS TIE: ZERO

FIGURE 12. CROSS-TIE MEMORY ELEMENT

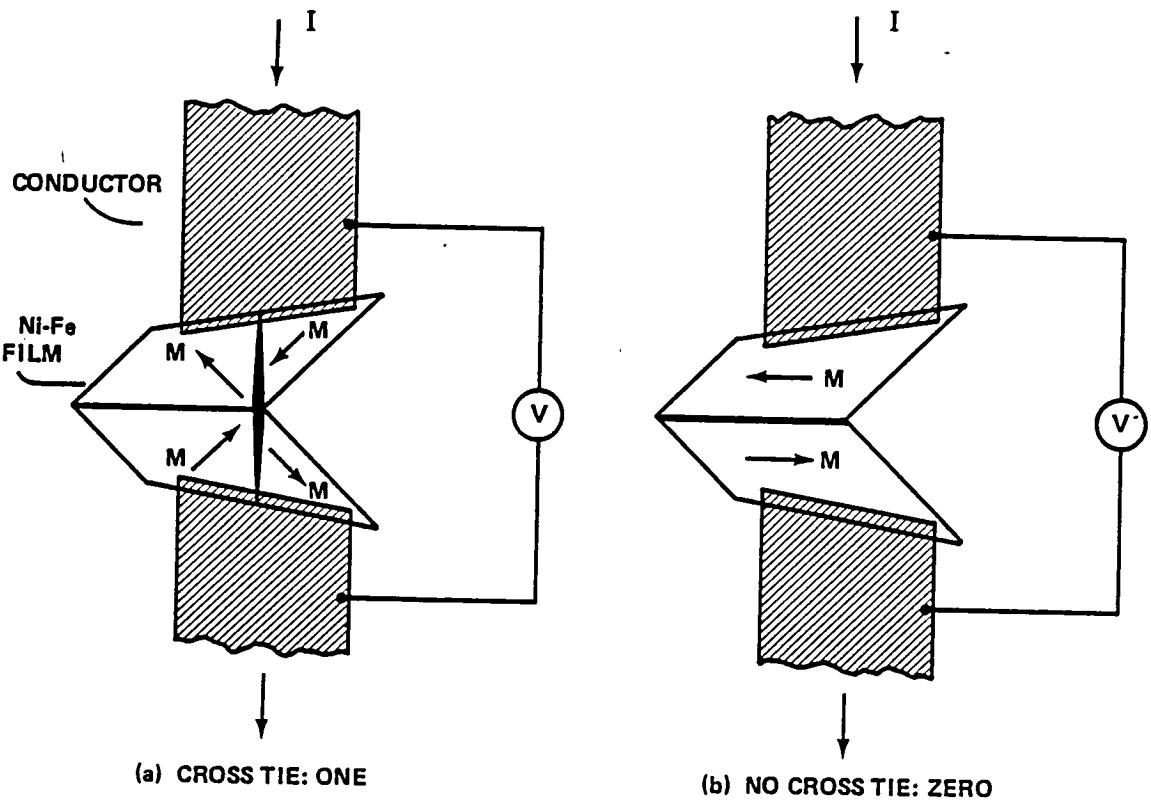
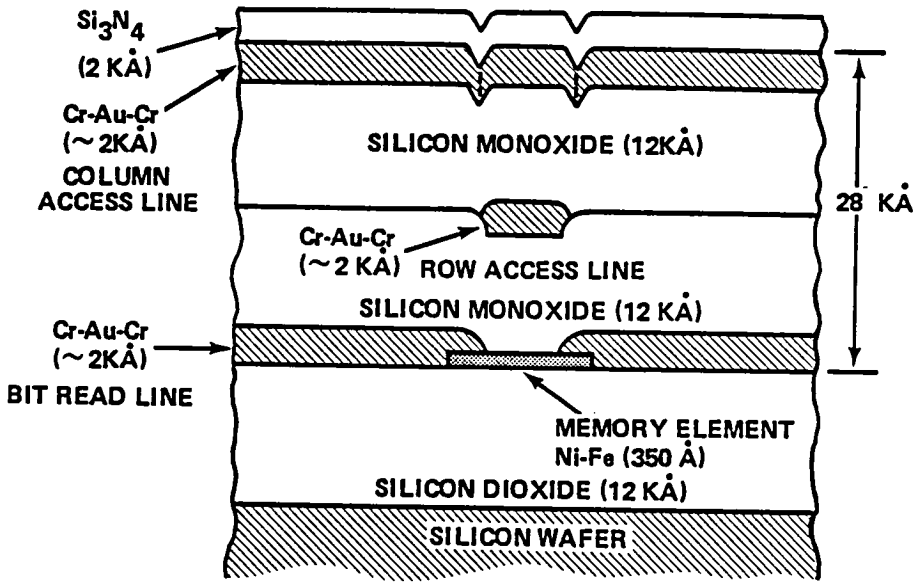



FIGURE 13. CROSS-TIE MAGNETORESISTIVE DETECTOR

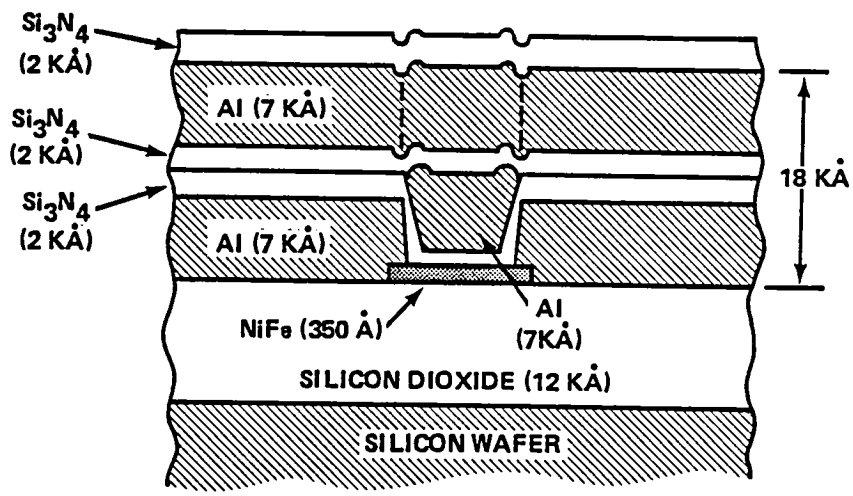
An entire memory cell consists of seven levels, as shown in Figure 14 (a), deposited on an oxidized silicon substrate. The first level is 350 Å of NiFe which is ion milled to form the memory elements as shown in Figures 12 and 15(a). The next level is 2000 Å of chromium–gold–chromium (Cr–Au–Cr) deposited directly onto the NiFe. This becomes the bit read (detector) lines as shown in Figure 15(b). Next comes a 12 KÅ insulating layer of silicon monoxide (SiO). This is followed by another 2000 Å layer of Cr–Au–Cr which is ion–milled to become the row access lines as shown in Figure 15(c). A second 12 KÅ SiO insulating layer is then deposited, followed by a third 2000 Å of Cr–Au–Cr. This layer becomes the column access lines as shown in Figure 15(d). The entire memory array is then coated with a 2000 Å passivating layer of silicon nitride ($Si_3N_4$). Figure 14(b) shows a similar cross section but using aluminum (Al) and $Si_3N_4$ for the metallization and insulating layers, respectively. Figure 15 shows the four individual metal layers that are part of a 16–bit experimental CRAM array. Figure 16 is a photograph of the actual device using the Cr–Au–Cr and SiO system as shown in Figure 14(a). Figures 17 and 18 show a partially populated 8K–bit chip and a test chip mounted on a leadless chip carrier.

To operate as a memory, the memory array must be coupled to various electronic circuits, in particular address decoders, line drivers, and sense amplifiers. The operation of the memory is quite simple. For a write cycle, the address is decoded and the proper row and column access lines are activated. Writing is done through a coincident current scheme, with the polarities of the currents dependent on whether a one or a zero is written. During a read cycle, the address is decoded and the appropriate row access and bit read lines are activated. The output of the bit read line is sampled while the read access line is pulsed. It is then fed into a sense amplifier, comparator, and latch before appearing as a transistor–transistor–logic level zero or one. Readout is nondestructive and the stored data are nonvolatile.

Sperry is developing a 16K x 1 CRAM chip that requires a single plus 5–volt supply. No power is needed for data retention. Power is used only when the chip is enabled. CRAM is based on a magnetic technology that implies infinite retention and unlimited write–read cycles. A preliminary design for such a chip is shown in Figure 19. Two magnetic arrays of 8K x 1 each are fabricated on the same silicon chip as the associated electronics. Cycle and access times are less than 500 nanoseconds and possibly as low as 100 to 200 nanoseconds. Operation of the CRAM is externally indistinguishable from a static semiconductor RAM except for the fact that the data are nonvolatile. No refresh is required. The CRAM has no permanent magnets or moving parts, and can therefore be integrated using standard semiconductor processing procedures. It operates over the full military temperature range of minus 55 to plus 125°C. This 16K chip can be used as the basis of a memory module to replace military core memory modules in such systems as AN/UYK–43, AN/UYK–44, AYK–15A, and F18. In addition, advanced versions of the CRAM may rival semiconductor memories in speed and density, opening up an entirely new range of applications in military and aerospace computer systems.

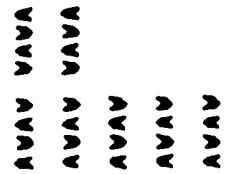



(a) Au-Cr/SiO STRUCTURE

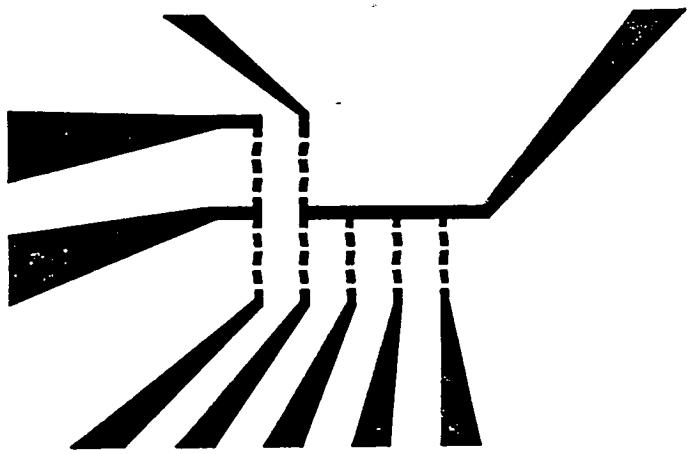



(b) Al/$Si_3N_4$ STRUCTURE

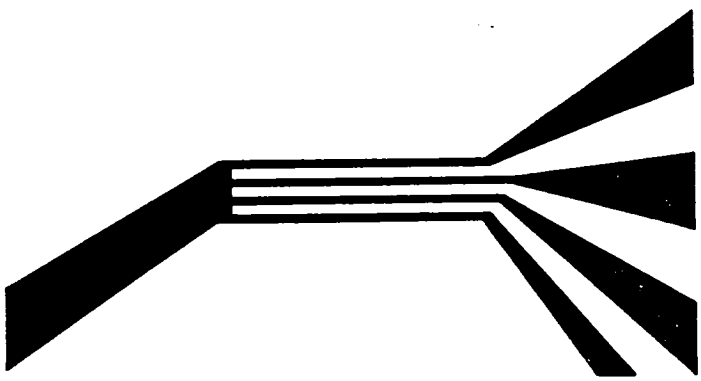
FIGURE 14. CROSS SECTION OF A CRAM CELL



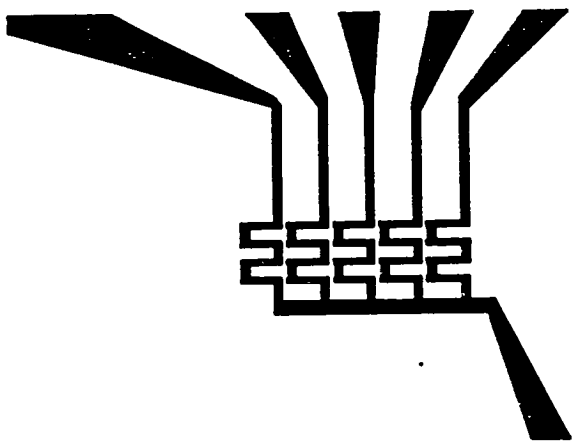
(a) MEMORY ELEMENT ARRAY



(b) BIT READ LINES



(c) ROW ACCESS READ AND WRITE LINES



(d) COLUMN ACCESS WRITE LINES

FIGURE 15. 16-BIT CRAM MAGNETIC AND CONDUCTIVE LAYERS

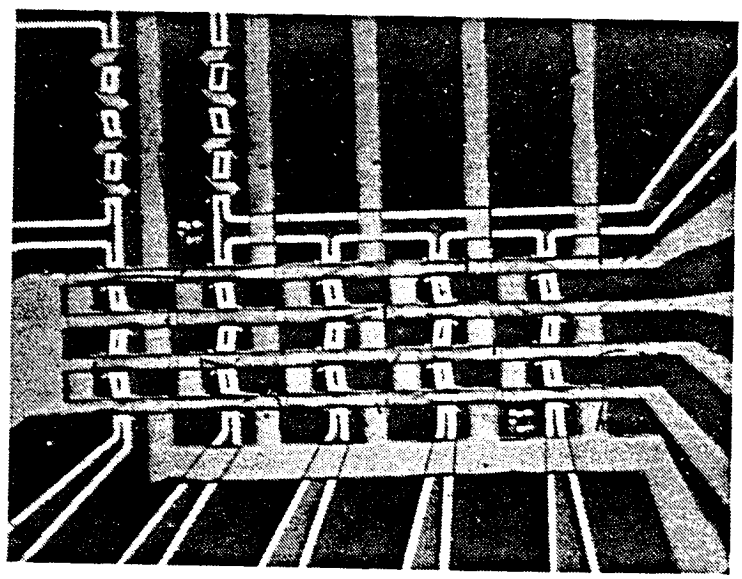


FIGURE 16. 16-BIT CRAM

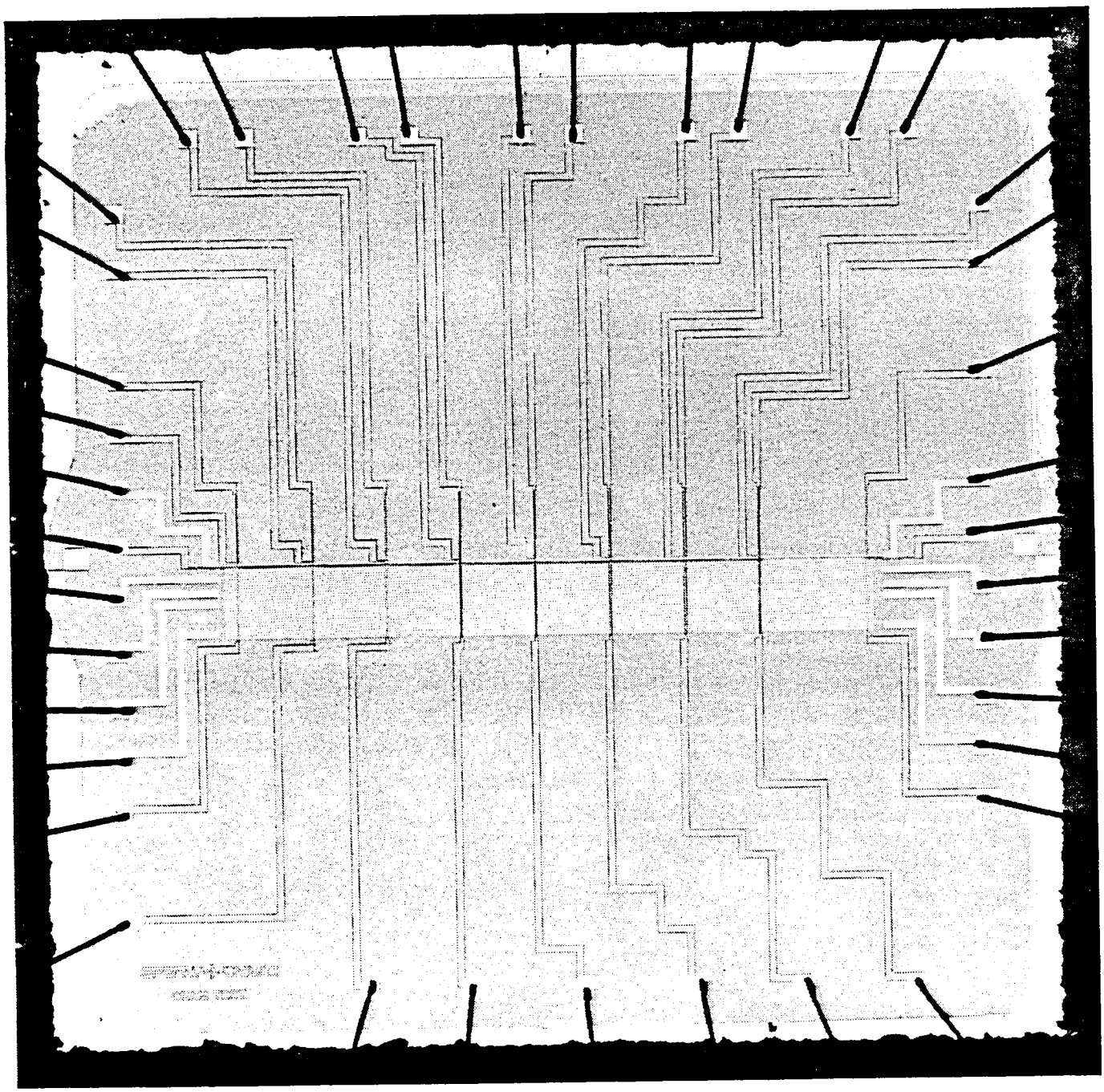


FIGURE 17. PARTIALLY POPULATED 8K (64 BY 128) CHIP

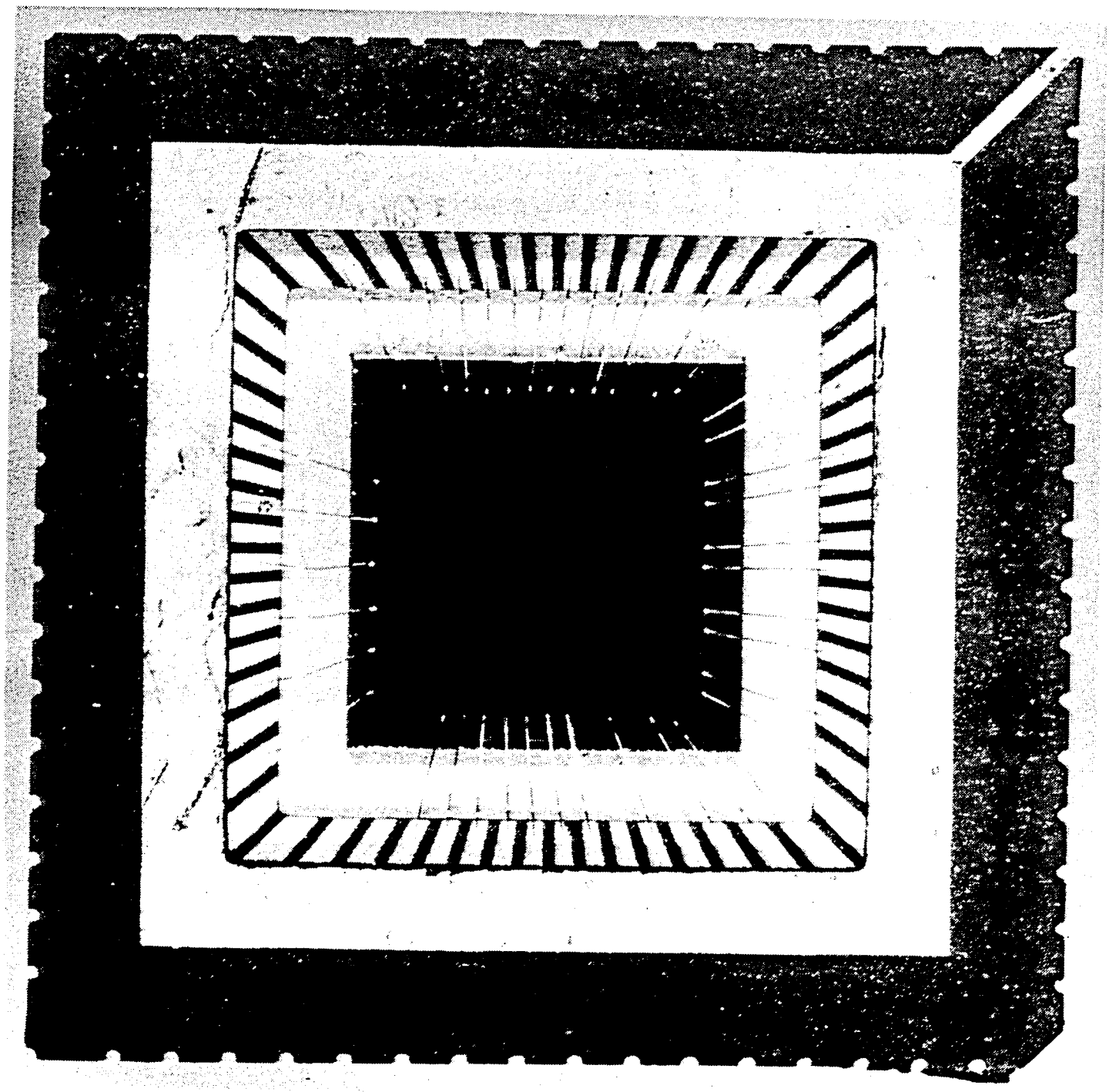


FIGURE 18. A TEST CHIP MOUNTED ON A LEADLESS CHIP CARRIER

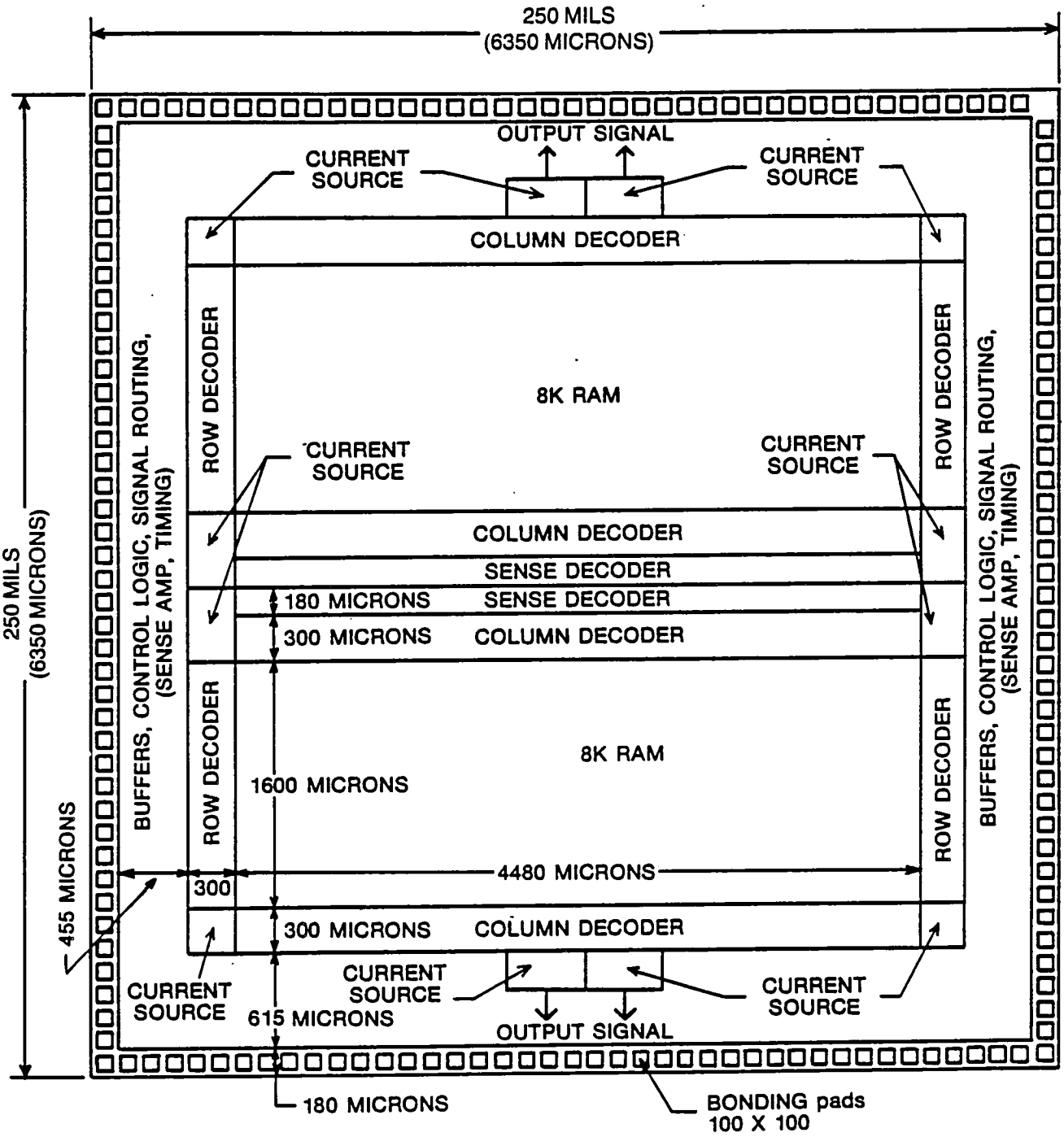



FIGURE 19. CROSS-TIE RAM LAYOUT FOR A 16K BY 1 CHIP

Cross-tie memory elements are made of polycrystalline NiFe films, which are intrinsically tolerant to radiation. The data storage mechanism does not depend on charge storage such as CCD, MNOS, or EEPROM nor on single crystalline substrates such as magnetic bubble, Ovshinsky devices, or thermomagnetic optical recording. Since the CRAM technology is still in its developmental stage, the effect of nuclear radiation has not been studied. However, based on the available data from tests on similar memory elements such as magnetic wire, magnetic film, and magnetic bubble, the CRAM element is expected to store data up to a neutron irradiation of $10^{16}$ neutrons per square centimeter, a total gamma dose of $5 \times 10^{7}$ rads (Si), and a gamma dose rate of $10^{12}$ rads (Si) per second for a 30-nanosecond half-pulse width.

As a conclusion for this section, Table 7 contains data on six memory technologies.

TABLE 7. MEMORY TECHNOLOGY

| TYPE / CHARACTERISTIC | CORE | CROSS TIE* | DYNAMIC RAM | MNOS BORAM | MAGNETIC BUBBLE | SELF-STRUCTURED BUBBLE* |
|---|---|---|---|---|---|---|
| Nonvolatile | Yes | Yes | No | Yes | Yes | Yes |
| Temperature | −55° to 85°C | −55° to 125°C | −55° to 125°C | −55° to 125°C | −40° to 85°C | −40° to 85°C |
| Write | 900 ns | 100 ns | 250 ns | 1 ms | 10 μs | 400 ns |
| Access time | 350 ns | 500 ns | 120 ns | 15 μs | 11.5 ms per 1 Mbit | 1 ms per 10 Mbit |
| Read (Data rate) | 900 ns | 500 ns | 250 ns | 500 ns (2 MHz) | 10 μs (100 KHz) | 400 ns (2.5 MHz) |
| Radiation hardened | Yes | Yes | No | No | Yes | Yes |
| Density (bits per chip) | 100K per plane | 16K | 64K | 8K | 1M | 10M |
| Price per bit | 1.5¢ | 0.06¢ | 0.04¢ | 0.4¢ | 0.05¢ | 0.004¢ |
| *Projected data | | | | | | |

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# APPENDIX C - MEMORY SYSTEM STUDY

Dennis Amundsen

## 1.Ø MEMORY SYSTEM REQUIREMENTS

To meet the goals of a nonvolatile spacecraft memory, the performance of a solid state memory must exceed that of current tape recorder memories. Using present recorders as a baseline, the desired characteristics of a solid state memory are summarized in Table 1.Ø. The performance of such a system would exceed that of current memory systems.

| | |
|---|---|
| Volume | <8ØØ $in^3$ (13110 $cm^3$; 1/2 ATR chassis) |
| Weight | <44.1 lb. (2Ø kg) |
| Capacity | >12Ø Mbit |
| Power | <7ØW at 1.2 Mbps |
| Data Rate | >1.2 Mbps |

TABLE 1.Ø

MEMORY MODULE REQUIREMENTS

Additionally, a solid state memory system should support both serial data recording and fast access to small blocks of data. An intelligent system controller would be necessary to implement write protection, host communication, and give the desired expansion flexibility.

### 1.1 Host Communication

Memory module communication with the host system(s) will be over a dual port interface. Each port will be identical, and have the capability of handling data independently, or alternating with the other port. Data, address, and handshake signal lines will form each parallel port. Additionally, each port provides a power strobe line (PSTROBE) to establish a minimum power condition. When inactive, PSTROBES removes all memory module power except that necessary to detect an active PSTROBE.

## 2.0 APPLICABLE TECHNOLOGIES

A solid state nonvolatile memory could be configured using a variety of technologies. However, to meet the density, power and data rate requirements only three general technologies are applicable. Each has its merits, which will be discussed in turn.

### 2.1 CMOS RAM with Battery

Volatile semiconductor RAM can retain stored data when used with a backup power source such as a battery. To minimize power drain during inactive periods, CMOS semiconductors are exclusively used. CMOS RAM provides extremely fast, truly random data access. Active power is also quite low. The necessary technology is widely available at reasonable cost. However, the use of battery backup delivers low nonvolatile store reliability. The volume and weight of the battery also reduces system capacity. Radiation susceptibility, already great in a MOS device, increases further during idle periods due to the lower supply voltage furnished by the backup battery. For these reasons, CMOS is not considered a viable memory technology, and will not be considered further.

### 2.2 EEPROM

Electrical erasurable PROMs (EEPROM) are inherently nonvolatile, eliminating the reliability problems associated with CMOS RAMs. However, they share the same radiation susceptibility problems as CMOS, which could be overcome only with unique radiation hardened processing techniques. This has been demonstrated for CMOS and MNOS technologies.

In the very near term, 64K bit EEPROMs in both CMOS and NMOS technologies will be available from several vendors. This density is the minimum necessary to approach capacity requirements of the memory module. At this

density, advanced packaging techniques such as multiple leadless chip carriers (LCC) on ceramic substrates would be used. The cost of the devices and the special packaging drives the system cost very high. Denser devices are projected in the near term (1-5 years), 128 Kbit devices in 1985, 256K by 1986 and 512 Kbit EEPROMs by 1988.1

1Electronic Engineering Times, Feb.13,1984, Issue 279 PP. 52-54

Due to the long write time of EEPROMs (Ø.2 ms to 1Ø ms/byte), many devices will be active during high speed store operations, with each active device in various stages of write completion. This can contribute to significant power consumption with NMOS devices. CMOS EEPROMs alleviate this problem with their much lower power requirements.

## 2.3 Bubble Memory

Bubble memory offers the possibility of dense memory systems at a low cost per bit. Of all the bubble device technologies, the classifications at each end of the performance scale were examined. Permalloy gap devices are lowest in performance, but are in wide use at the present. Self-structured current access devices offer the highest performance, but are currently in the research stage with practical implementation many years away.

### 2.3.1 Permalloy Field Access Devices

Permalloy field access bubble memory devices are characterized by permalloy magnetic features laid on the garnet material to define data storage areas. Field coils produce a rotating field to propagate bubbles through the device and to a detector output(s). These devices are presently being used in commercial and military products. Current densities are at 1 mbit per

device, with 4 mbit devices available soon. Bubble memory has and will maintain a significant cost per bit advantage over other technologies[1].

Power requirements for a suitable bubble memory are relatively high. This is due to the necessity of operating several devices in parallel to increase the data rate. Presently, commercial devices are limited to a data transfer rate of approximately 100 kbps. The use of multiple detector outputs in the 4 mbit devices will increase the data rate by a factor of four, reducing the needed number of parallel devices, Table 2.1.

### 2.3.2 Self-Structured Current Access Devices

Self-structured current access bubble devices do not rely on external magnetic features to define bubble tracks, therefore yielding a higher density than permalloy types. The absence of propagating field coils reduces power requirements and increases data transfer rate. Such a device is still in the research stage with system implementation practical only in the long term (5-8 years). However, a comparison with permalloy types give a good indication of bubble memory trends for the future.

## 3.0 SYSTEM CONFIGURATION

Each memory system unit is a single 1/2 ATR avionics chassis (9.75 in. X 10.12 in. X 7.6 in.). Multiple memory modules may be connected to a common external bus. Contained within the chassis are two printed circuit cards dedicated to I/O and memory control, a number of memory cards, and a power supply. The number of memory cards can vary with the chosen technology and desired capacity.

Each PC card is a standard 6.3 inches by 9 inches. All cards use thermally

| | CAPACITY | PEAK DATA RATE | # OF PARALLEL DEVICES FOR AVERAGE 1.4 Mbps | SINGLE DEVICE POWER |
|---|---|---|---|---|
| Motorola | 1 M | 100 khz | 16 | 1.9 W |
| Fujitsu | 1 M | 100 khz | 16 | 1.3 W |
| | 4 M | 400 khz | 4 | 3.8 W |
| Intel | 1 M | 100 khz | 16 | 1.3 W |
| | 4 M | 400 khz | 4 | 2.9 W |



TABLE 2.1

PERMALLOY BUBBLE DEVICES POWER AND DATA RATES

conductive heat ladders to transfer component heat to the card edges. Wedge clamps secure each card in the chassis, ensuring efficient heat conduction from the cards. A finned chassis surface and/or mounting on a suitable heat sink surface allows for a completely conduction cooled system.

The choice of memory technology, by virtue of density and power requirements, affect the module capacity, power, and weight. Possible system configurations for several technologies are presented, with greater detail given for the more viable candidates.

### 3.1 CMOS RAM and EEPROM Implementations

While CMOS RAM with battery backup has previously been deemed unacceptable, its density, packaging and power requirements are equivalent to CMOS EEPROM. The system description which follows for an EEPROM configuration is therefore valid for CMOS RAM also, with the exception of the backup battery.

To achieve the highest system capacity with near term 64 kbit components, high density packaging methods were examined. Mounting LCC memory chips on both sides of a ceramic substrate, Figure 3.1, in turn mounted on a PC card, allowed achievement of reasonable system capacity. Two substrate configurations were examined to achieve maximum density.

#### 3.1.1 Dual-In-Line Package (DIP) Implementation

A ceramic substrate with six LCCs can be configured as a large DIP (2.5 inches, 48 pins) with Ø.6 inch lead spacing. Such techniques are presently used in avionics equipment. Each DIP straddles a heat rail, which by physical contact carries heat to the card edges. Such mounting results in 18 substrates per PC card for a total of 1Ø8 64K memory chips (Figure 3.2).

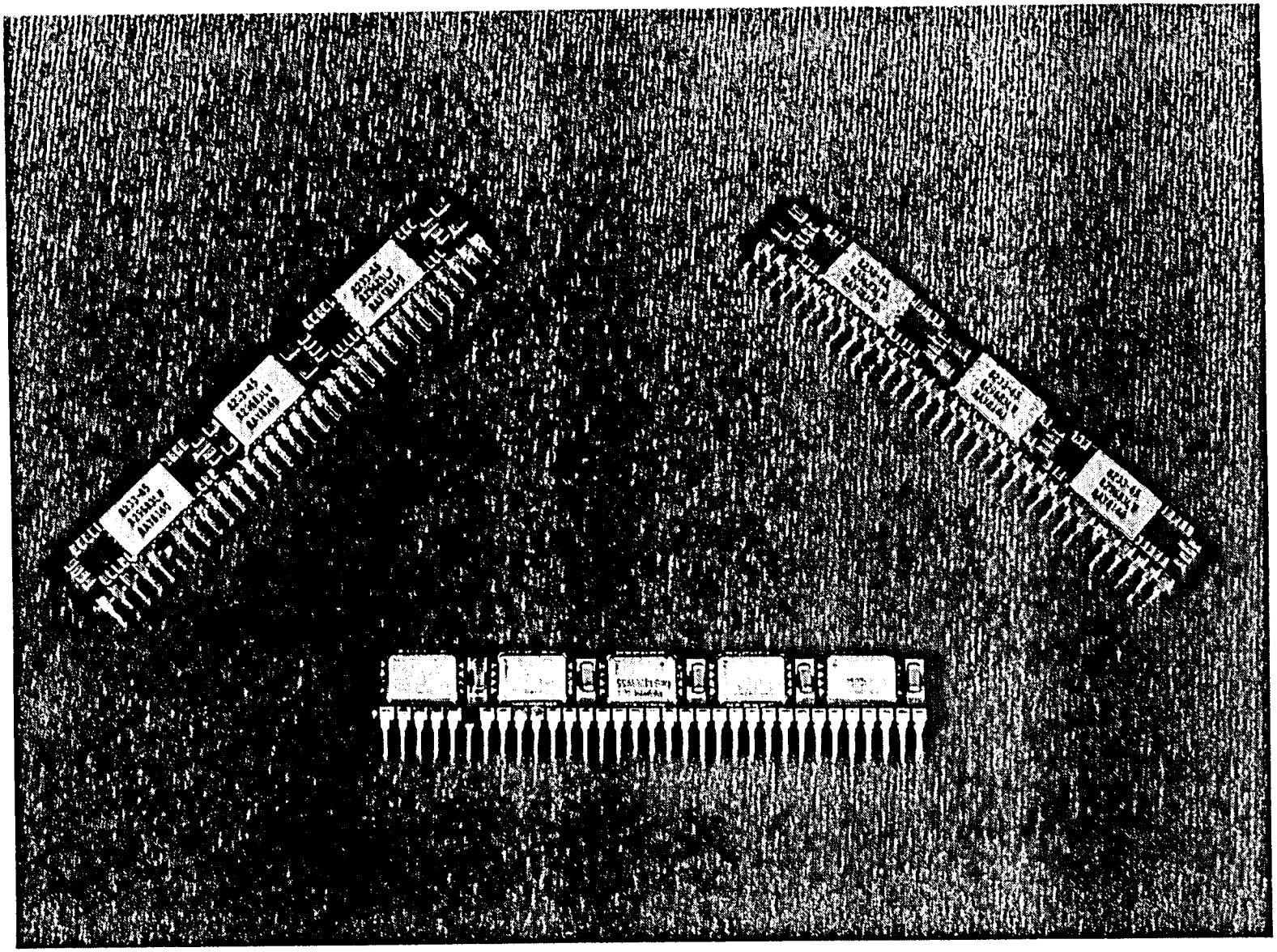


**FIGURE 3.1 LEADLESS CHIP CARRIER ON CERAMIC SUBSTRATE PACKAGING**

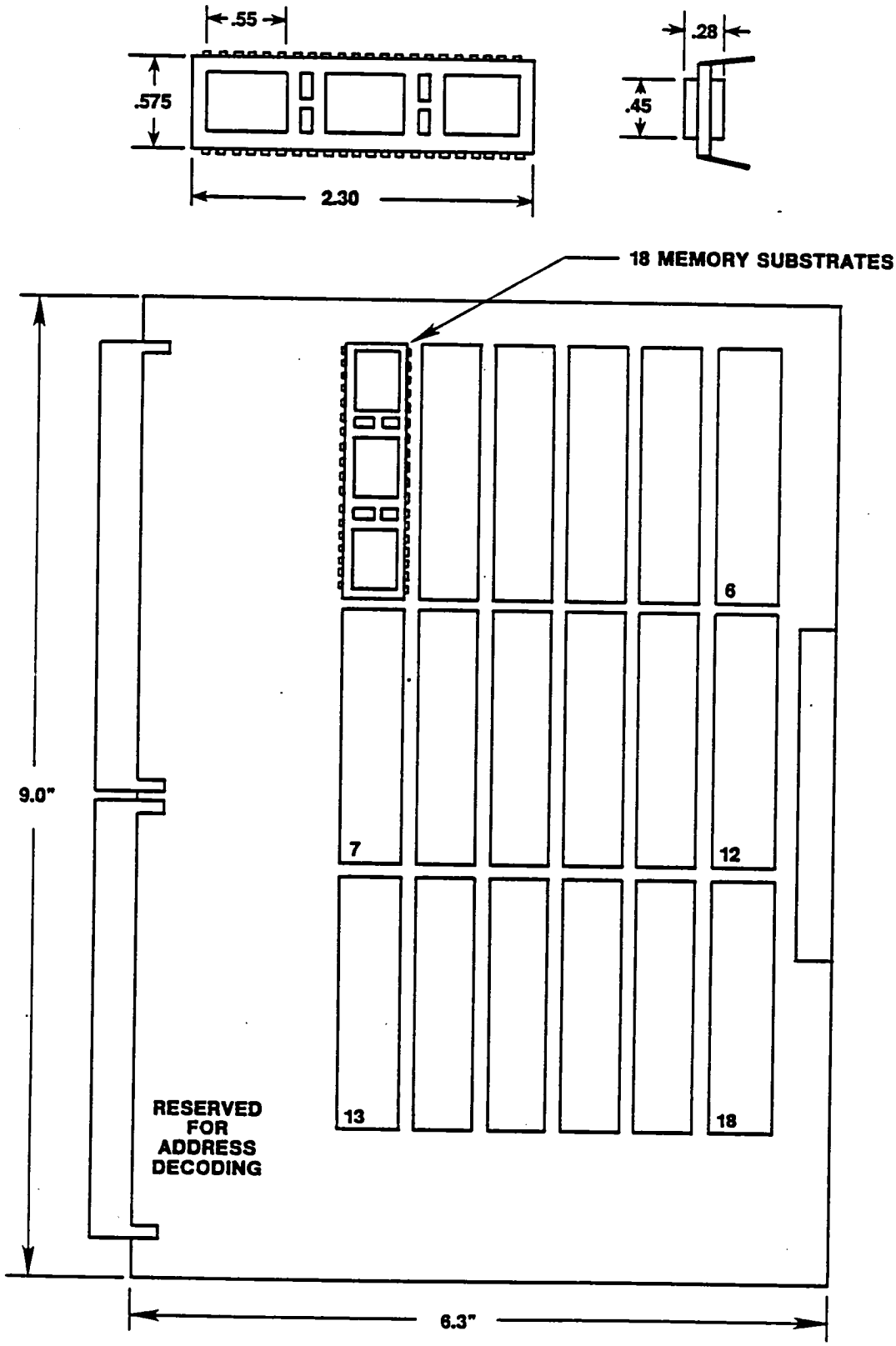



FIGURE 3.2. $E^2$PROM DIP MEMORY CARD LAYOUT

The resultant component and board height of Ø.4 inches allows mounting of the memory cards on Ø.5 inch centers. A maximum of 11 memory cards could reside within the chassis for a capacity of 76 mbits (Figure 3.3).

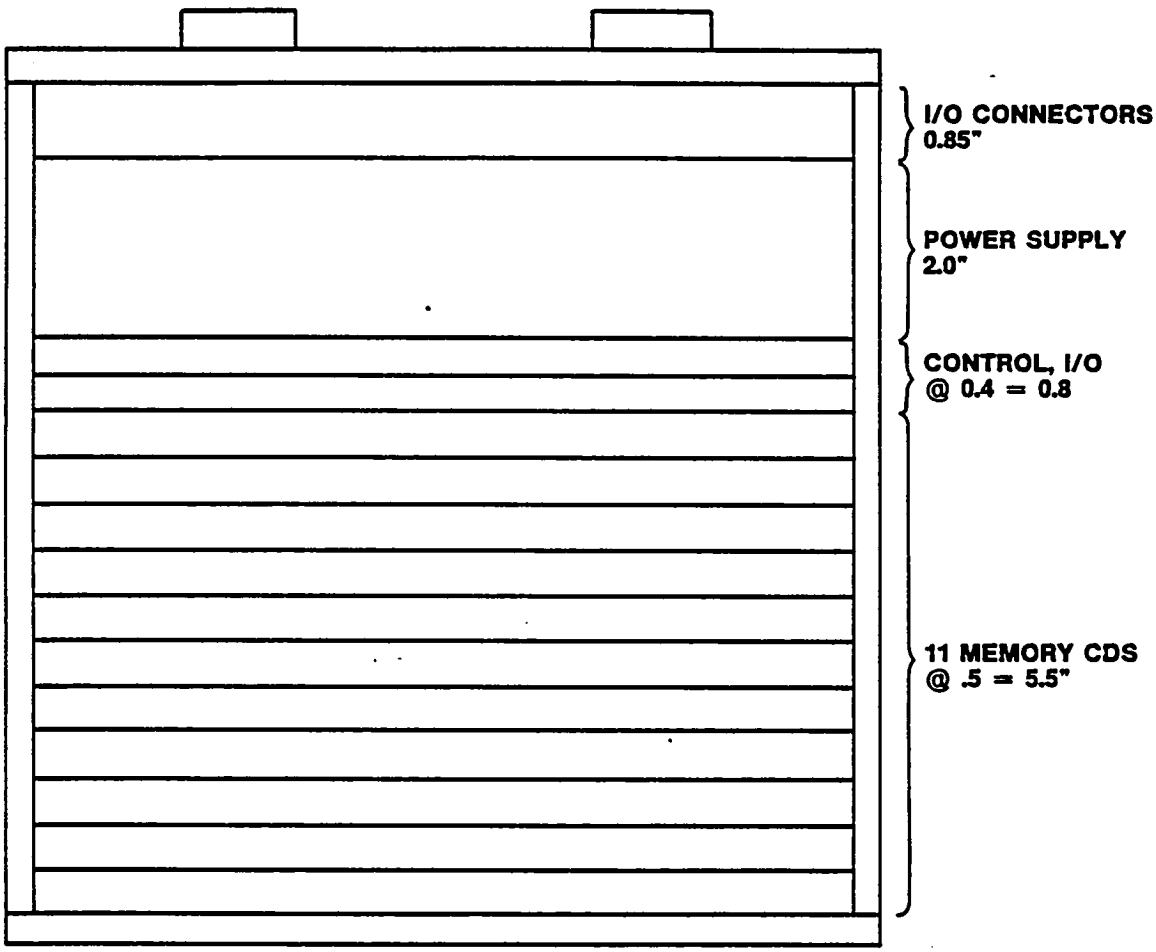
### 3.1.2 Vertical DIP (VDIP) Implementation

A ceramic substrate with six LCCs can be mounted in a vertical configuration to achieve higher density (Figure 3.4). Each substrate has two rows of 2Ø pins, each row separated by Ø.1 inch. Such a scheme allows 34 substrates containing 2Ø4 64K memory chips per PC card. Total card ehight of Ø.725 inches allows mounting of the memory cards on Ø.8 inch centers. A maximum of seven memory cards can reside within the chassis for a capacity of 91.4 mbits (Figure 3.5).

Vertical mounting of the substrate carriers require support on each end to withstand vibration and for heat conduction. Three aluminum rails with spring wedge clamps running longitudinally on the PC card would serve these purposes. Since this mounting technique approaches the desired capacity, an in-depth look is appropriate.

### 3.1.3 64K EEPROM Devices

The characteristics of several 64K bit EEPROM devices from various vendors are listed in Table 3.1. A 32K bit device is also shown for comparison purposes. CMOS and various NMOS process technologies are used. CMOS EEPROM devices, a recent entry to the field, exhibit low operating power and extremely low standby power. Write times have been improved over lower density devices, with a new range of Ø.2 to 1.Ø milliseconds. This higher speed has been achieved through the use of a page write mode, with the




108 64K CHIPS/CARD = 6.9 M/CD
11 CDS = 76.0 MBIT

FIGURE 3.3. $E^2$PROM (DIP) MEMORY CHASSIS LAYOUT

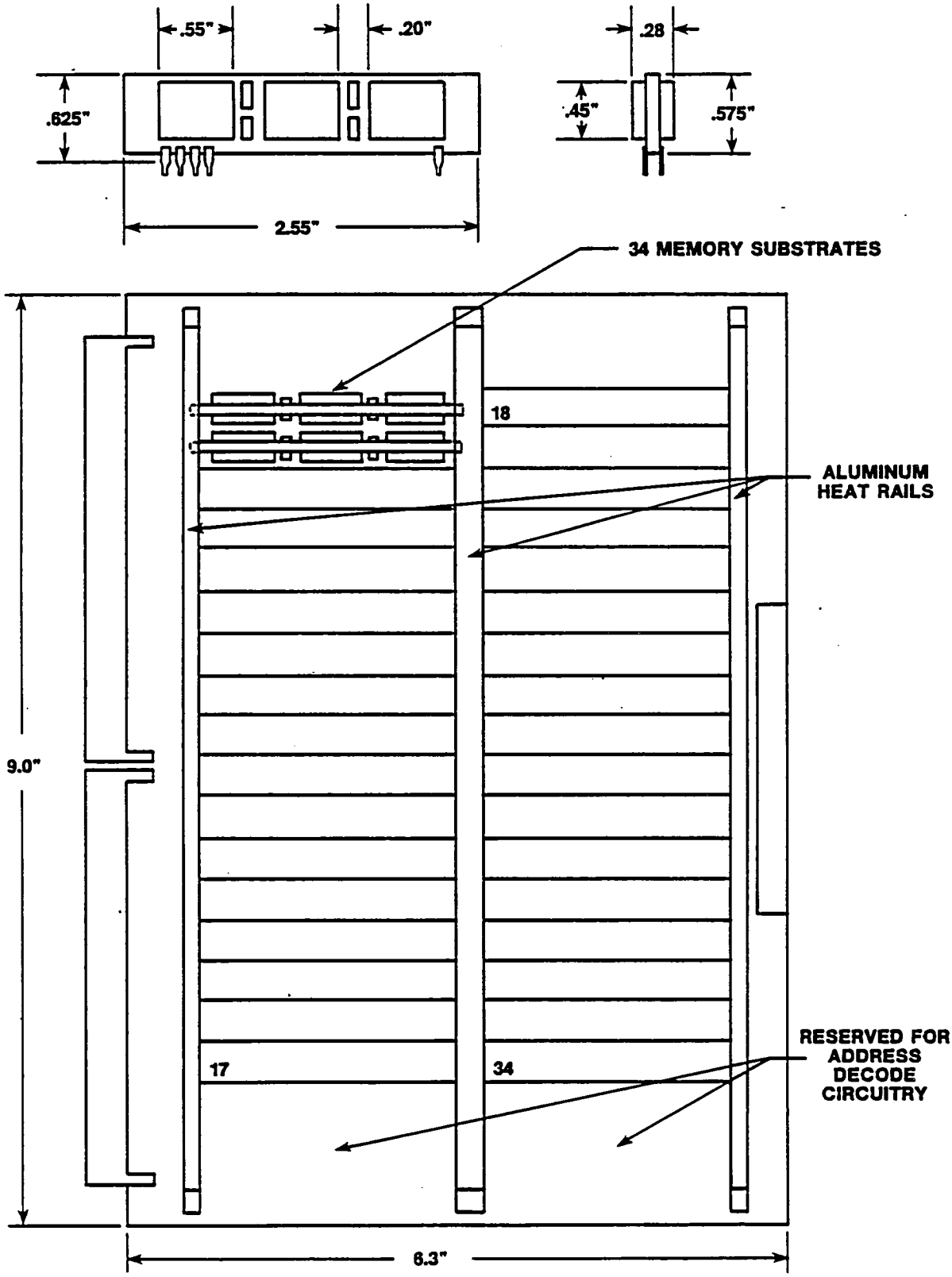
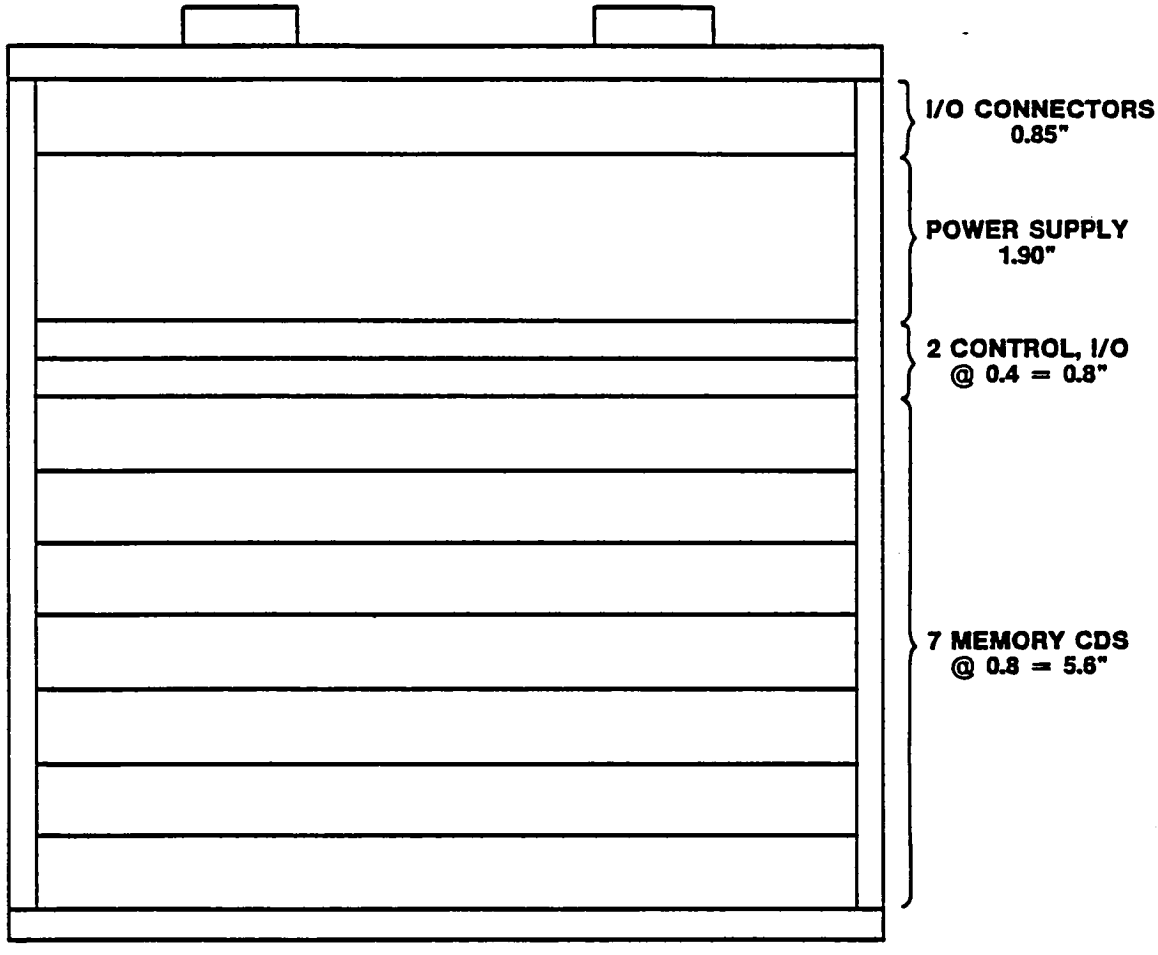



FIGURE 3.4. $E^2$PROM VIP MEMORY CARD LAYOUT




**204 64K CHIPS/CARD = 13.1 MBIT/CD 7 CDS = 91.4 MBIT**

**FIGURE 3.5. $E^2$PROM VDIP MEMORY CHASSIS LAYOUT**

| VENDOR | PART NO. | PROCESS TECHNOLOGY | SIZE | POWER (MW) ACTIVE | POWER (MW) STANDBY | WRITE TIME PER BYTE (MS) | AVAILABILITY |
|---|---|---|---|---|---|---|---|
| EXEL | 48C64 | CMOS | 8K X 8 | 25 | .005 | .4* | SAMPLES |
| HUGHES | 3164 | CMOS F.G. | 8K X 8 | 10 | 0.25 | --- | SAMPLES |
| AMD | 9864 | NMOS F.G. | 8K X 8 | 350 | 100.0 | --- | SAMPLES |
| INMOS | 3630 | NMOS | 8K X 8 | 750 | 100.0 | 0.2* | SAMPLES |
| NCR | 52832 | SNOS | 4K X 8 | 300 | 150.0 | 0.6* | PRODUCTION |
| SEEQ | 5233 | NMOS F.G. | 8K X 8 | 300 | 90.0 | 1.0 | SAMPLES |
| XICOR | 2864 | NMOS F.G. | 8K X 8 | 550 | 250 | 0.3* | SAMPLES |

*PAGE WRITE MODE

FIGURE 3.1. HIGH DENSITY EEPROMS

exception of the SEEQ 5233 device. Page mode allows the input at high speed of 16 to 64 bytes into internal latches, followed by a parallel write of the latch contents into the memory. Thus the normally long write cycle is reduced by a factor equal to the buffer length.

### 3.1.4 Power Requirements

System power for an EEPROM memory system is data rate dependent. This factor is most pronounced during writes due to the slow write time of EEPROMs. With current devices, the effective (accounting for page mode) byte write time may range from 0.2 ms to 10 ms. Once a single device is written, it must be allowed to complete its write cycle. Therefore, during high speed writes, successive bytes or pages of bytes must be written to different devices, creating a large number of active devices as shown in Figure 3.6. The high speed read capability (<400 nanoseconds) of EEPROMs avoids this problem during read operations, with all devices inactive over 99% of the time.System active power calculations for an EEPROM memory based on various vendor devices are shown in Table 3.2. The power has been calculated at various data rates for a 100% duty cycle. Power gating of the entire system with PSTROBE (See 1.1) would reduce the powers shown by a factor equal to the duty cycle. Power for write operations is shown, with memory read power equal to the zero data rate powers. Calculations are based upon the density achieved with vertical DIP substrates, 204 devices per card, with power gating of unused cards. Only one memory card has power applied at any given time. All devices on the single active card must have power applied (some devices active, others on standby) to meet the high data rate during writes (175 of the 204 devices may be active). Controller and I/O power was assumed at 15 watts. Primary input power was calculated assuming a realistic power supply efficiency of 65%.

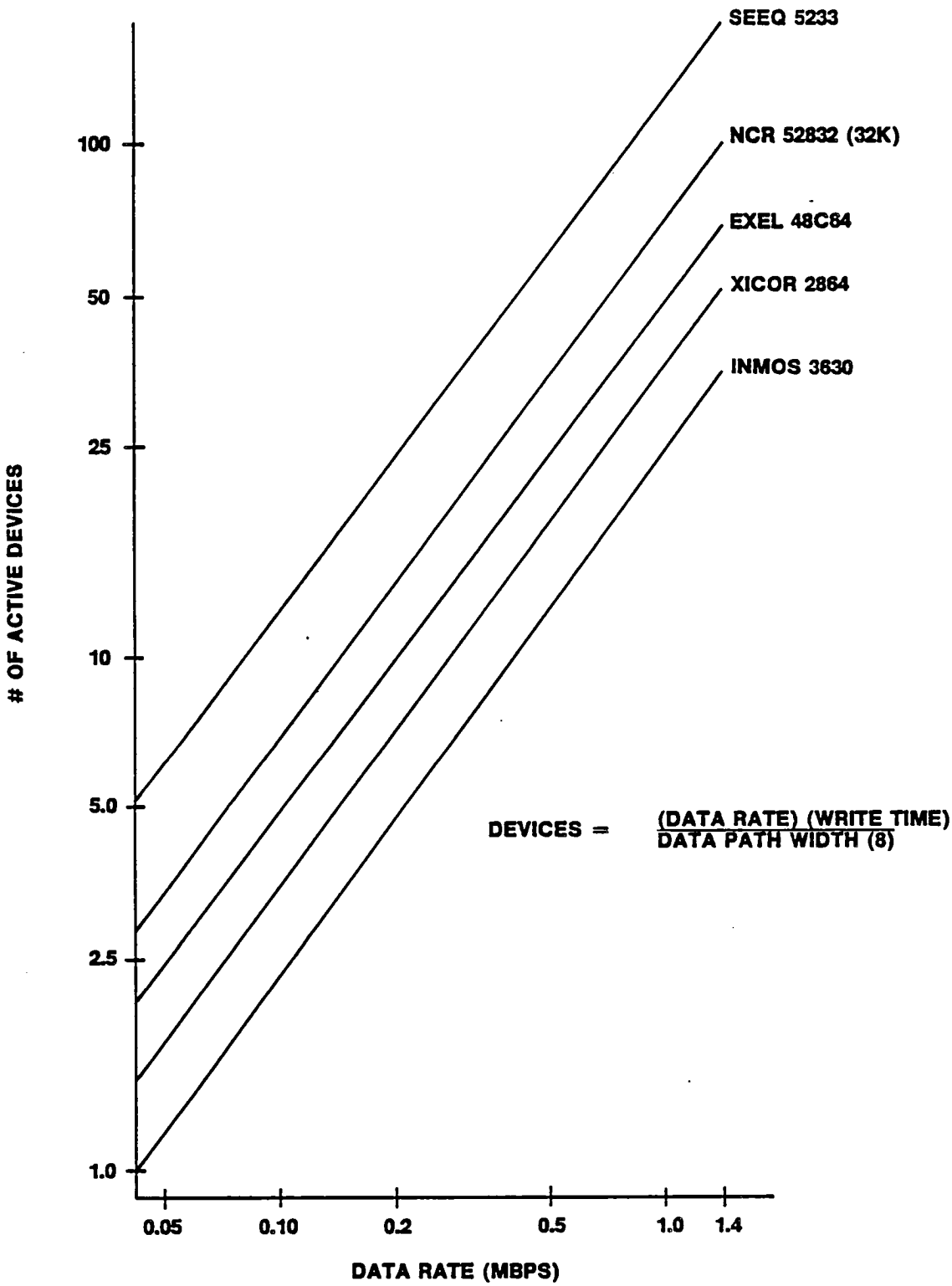



FIGURE 3.6. # OF ACTIVE DEVICES DURING WRITES

| DATA RATE (MPBS) | # OF ACTIVE DEVICES (WRITE) | ACTIVE DEVICE POWER | INACTIVE DEVICE POWER | CONTROL CD & I/O POWER | SECONDARY POWER | PRIMARY INPUT POWER |
|---|---|---|---|---|---|---|
| SEEQ 5233 NMOS | 1 MS/BYTE ACT | 300 mW/DEVICE ACT *0.3 | 90 mW/DEVICE (204-ACT)*.09 | | | n = 65% |
| 1.4 | 175.0 | 52.50W | 2.61W | 15W | 70.11W | 107.86W |
| 1.0 | 125.0 | 37.50W | 7.11W | 15W | 59.61W | 91.71W |
| 0.5 | 62.5 | 18.75W | 12.74W | 15W | 46.49W | 71.52W |
| 0.1 | 12.5 | 3.75W | 17.24W | 15W | 36.00W | 55.38W |
| 0.05 | 6.25 | 1.88W | 17.80W | 15W | 34.68W | 53.35W |
| 0.01 | 1.25 | 0.38W | 18.25W | 15W | 33.63W | 51.74W |
| 0.0 (READ) | 0.0 | 0.0 | 18.36W | 15W | 33.36W | 51.32W |
| NCR 52832 SNOS (32K) | PAGE MODE 0.6 ms/byte | 300 mW/DEVICE | 150 mW/DEVICE | | | |
| 1.4 | 105.0 | 31.50W | 14.85W | 15W | 61.35W | 94.39W |
| 1.0 | 75.0 | 22.50W | 19.35W | 15W | 56.85W | 87.46W |
| 0.5 | 37.5 | 11.25W | 24.98W | 15W | 51.23W | 78.82W |
| 0.1 | 7.5 | 2.25W | 29.48W | 15W | 46.73W | 71.89W |
| 0.05 | 3.75 | 1.13W | 30.04W | 15W | 46.17W | 71.03W |
| 0.01 | 0.75 | 0.23W | 30.49W | 15W | 45.72W | 70.34W |
| 0.0 (READ) | 0.0 | 0.0 | 30.60W | 15W | 45.60W | 70.15W |

*PSTROBE Active

TABLE 3.2-A. EEPROM SYSTEM POWER REQUIREMENTS

| DATA RATE (MPBS) | # OF ACTIVE DEVICES (WRITE) | ACTIVE DEVICE POWER | INACTIVE DEVICE POWER | CONTROL CD & I/O POWER | SECONDARY POWER | PRIMARY INPUT POWER |
|---|---|---|---|---|---|---|
| XICOR 2864 NMOS | 1 PAGE MODE 0.3 ms/BYTE | 550 mW | 250 mW | | | n = 65% |
| 1.4 | 52.5 | 28.88 | 37.88W | 15W | 81.76W | 125.78W |
| 1.0 | 37.5 | 20.63 | 41.63W | 15W | 77.26W | 118.86W |
| 0.5 | 18.75 | 10.31W | 46.31W | 15W | 71.62W | 110.18W |
| 0.1 | 3.75 | 2.06W | 50.06W | 15W | 67.12W | 103.26W |
| 0.05 | 1.88 | 1.03W | 50.53W | 15W | 66.56W | 102.40W |
| 0.01 | .38 | .21W | 50.91W | 15W | 66.12W | 101.72W |
| 0.0 (READ) | 0.0 | 0.0 | 51.00W | 15W | 66.00W | 101.54W |
| INMOS 3630 MNOS | PAGE MODE 0.2 ms/BYTE | 750 mW | 100 mW | | | |
| 1.4 | 35.0 | 26.25W | 16.90W | 15W | 58.15W | 89.46W |
| 1.0 | 25.0 | 18.75W | 17.90W | 15W | 51.65W | 79.46W |
| 0.5 | 12.5 | 9.38W | 19.15W | 15W | 43.53W | 66.97W |
| 0.1 | 2.5 | 1.88W | 20.15W | 15W | 37.03W | 56.97W |
| 0.05 | 1.25 | 0.94W | 20.28W | 15W | 36.22W | 55.72W |
| 0.01 | .25 | .19W | 20.38W | 15W | 35.57W | 54.72W |
| 0.0 (READ) | 0.0 | 0.0 | 20.40W | 15W | 35.40W | 54.46W |

*PSTROBE ACTIVE

FIGURE 3.2-B. EEPROM SYSTEM POWER REQUIREMENTS

| DATA RATE (MPBS) | # OF ACTIVE DEVICES (WRITE) | ACTIVE DEVICE POWER | INACTIVE DEVICE POWER | CONTROL CD & I/O POWER | SECONDARY POWER | PRIMARY INPUT POWER |
|---|---|---|---|---|---|---|
| EXEL 48C64 CMOS | PAGE MODE 0.4 ms/BYTE | 25 mW | .005 mW | | | n = 65% |
| 1.4 | 70.0 | 1.75W | NEGLIGIBLE | 15W | 16.75W | 25.77W |
| 1.0 | 50.0 | 1.25W | | 15W | 16.25W | 25.00W |
| 0.5 | 25.0 | 0.63W | (7 mW) | 15W | 15.63W | 24.05W |
| 0.1 | 5.0 | 0.13W | | 15W | 15.13W | 23.28W |
| 0.05 | 2.5 | 0.06W | | 15W | 15.06W | 23.17W |
| 0.01 | 0.5 | 0.01W | | 15W | 15.01W | 23.09W |
| 0.0 | 0.0 | 0.0W | | 15W | 15.00W | 23.08W |

*PSTROBE ACTIVE

FIGURE 3.2-C. EEPROM SYSTEM POWER REQUIREMENTS

The resulting power calculations of Table 3.2 are plotted in Figure 3.7. System power at 1.4 Mbps ranges from 26 to 125 watts among the various devices, with a mean power of 88 watts. The main factors influencing the system power characteristics are the EEPROM device active power, standby power and effective byte write time.

### 3.1.5 Weight Estimates

A weight breakdown of a complete 1/2 ATR 91.4 mbit EEPROM memory module chassis is shown in Table 3.3 for both DIP and VDIP configurations. Total weights are 28.9 lbs. and 27.3 lbs. respectively. The additional weight of the DIP configuration is due to the increased number of PC cards, each with a lower density than the VDIP scheme.

## 3.2 Bubble Memory Implementations

The use of permalloy or self-structured bubble devices yield similar systems with respect to controller complexity, number of PC cards, and bubble support circuitry. Memory capacity, data rate and power directly reflect the characteristics of the two device types.

### 3.2.1 Permalloy Implementation

To achieve the desired system capacity using current 1 mbit devices, LCC packaging must be used on much of the bubble support electronics. With such techniques, 16 bubble devices and all required support circuitry can reside on one standard 6.3 inch by 9 inch PC card (Figure 3.8). All sense amps, operation current drivers, and coil drivers with their associated low noise detection or high currents are isolated to the card, allowing only digital signals to be passed off the card. PROMs are also on the card, holding a permanent record of the redundant loop information of the devices. All

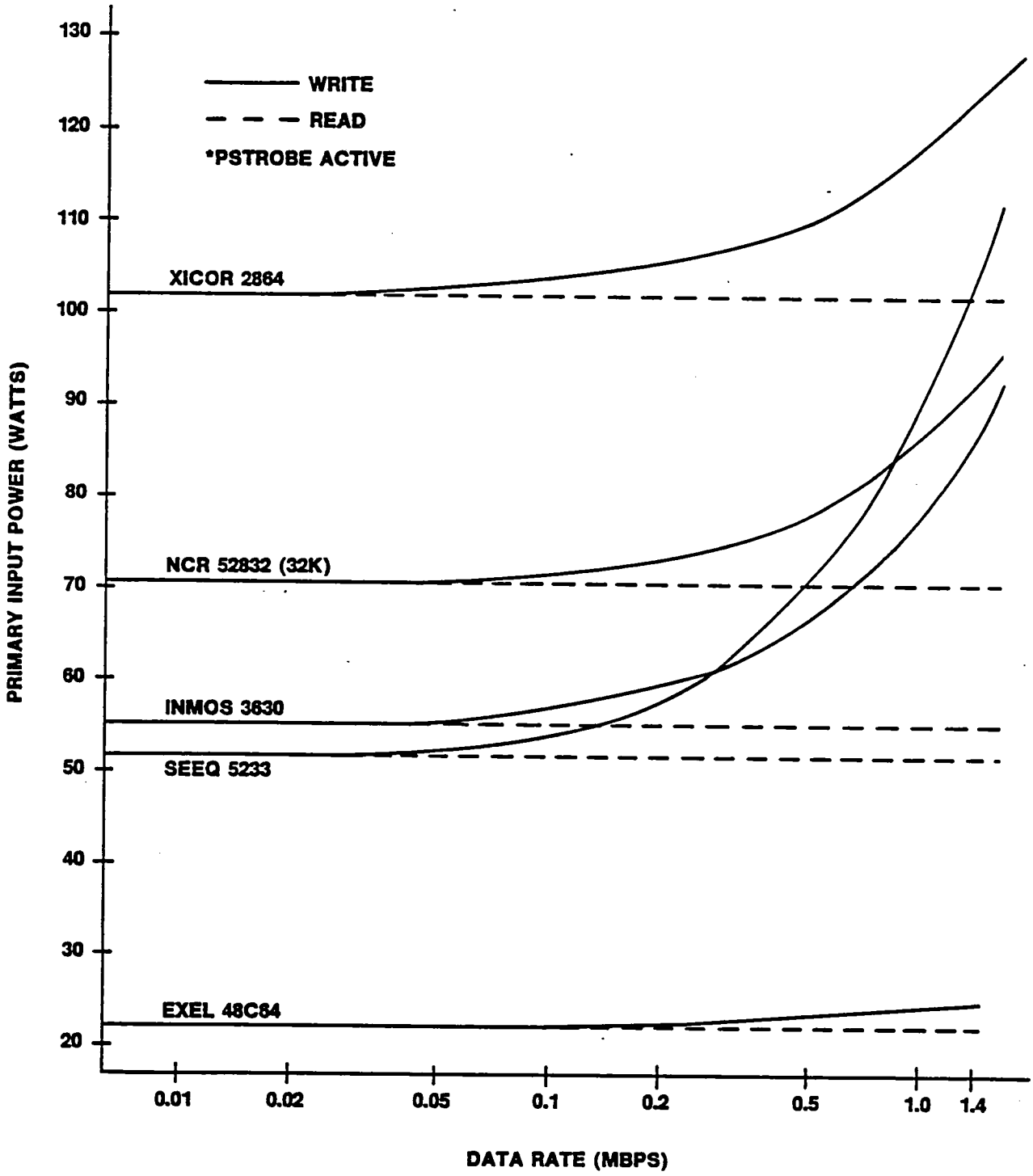



FIGURE 3.7. SYSTEM INPUT POWER INCREASES WITH DATA RATE

| EQUIPMENT BREAKDOWN | UPRIGHT DIP CONFIGURATION | DIP CONFIGURATION |
|---|---|---|
| Total | 27.3 | 28.9 |
| Chassis | 10.19 | 10.19 |
| Front | .786 | .786 |
| Back | .874 | .874 |
| Sides | 1.940 | 1.940 |
| Cover Top | 1.174 | 1.174 |
| Cover Bottom | 1.532 | 1.532 |
| Hardware | .490 | .490 |
| Wedge Clamps | 1.454 | 1.454 |
| Motherboard | 1.21 | 1.21 |
| PC Board | .742 | .742 |
| Pins | .468 | .468 |
| I/O | .29 | .29 |
| Connectors | .229 | .229 |
| Wiring & Cables | .059 | .059 |
| PC Cards | 12.59 | 14.27 |
| Heat Ladder | .133 | .133 |
| Connectors (2 100 pin) | .082 | .082 |
| PC Board | .407 | .407 |
| Components | | |
| Control Cards (2) | .309 | .309 |
| Memory Cards (7) | .847 | (11) .448 |
| Conformal Coat | .049 | .049 |
| Power Supply | 3.00 | 3.00 |

TABLE 3.3

$E^2$PROM MEMORY MODULE WEIGHT BREAKDOWN

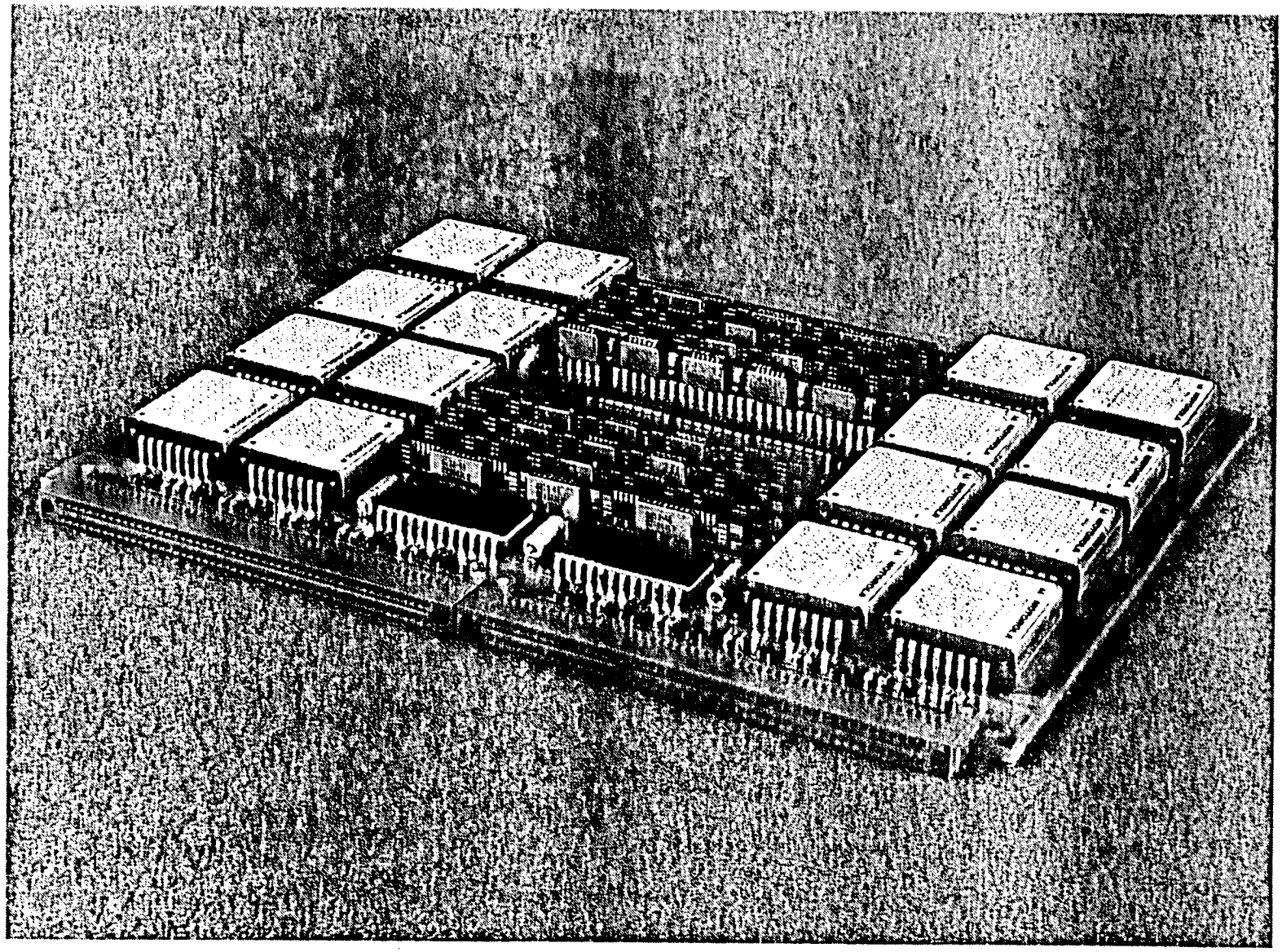


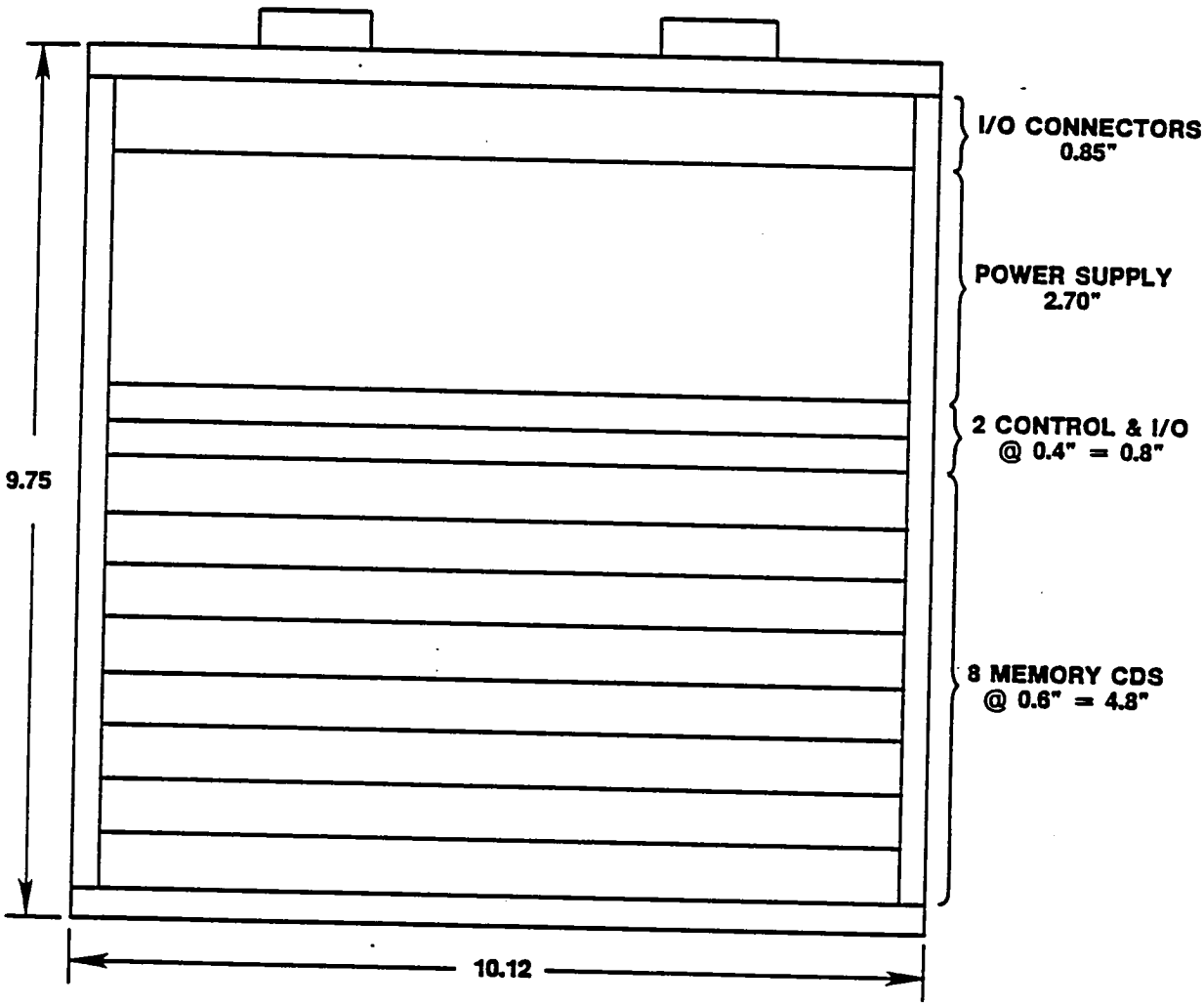
**FIGURE 3.8 16 MBIT BUBBLE MEMORY CARD ACHIEVED WITH HIGH DENSITY PACKAGING**

sixteen devices are operated simultaneously in parallel to increase the data transfer rate. With each device operating at a maximum of 100 Kbps, the total average transfer rate is 16*100K*.875 = 1.4 Mbps, which is reduced from the maximum by the redundant loops.

Memory cards are mounted on 0.6 inch centers, allowing eight cards per chassis for a capacity of 128 mbits, Figure 3.9. Each card is power-gated, therefore only a single card is in operation for data transfers to reduce power requirements. Use of 4 mbit devices increases capacity and reduces power. Replacement of costly LCC with conventional DIPs reduces the number of bubble devices in the system by one half, but still yields 256 mbits. Retention of the LCC packaging approach yields a 512 mbit capacity.

### 3.2.2 Self-Structured Implementation

Although the use of self-structured devices is years away, the characteristics of such a device can be safely projected. For incorporation into this system, a chip capacity of 8 mbits within approximately the same physical size as permalloy types was assumed. Data rate was assumed as 1.4 Mbps, achievable through multiple chips or I/O ports per device. An operating power of 0.5 W per device was used. These assumptions are conservative on the potential of self-structured devices. A self-structured device requires support circuitry similar to permalloy types, sense amplifiers, current generators, timing control, etc. Using conventional packaging of the support electronics, it is estimated that a system capacity of 384 mbits could be achieved with 8 memory cards of 8 devices each. Higher capacity could be with denser packaging techniques. A primary advantage of using self-structured devices is power reduction. The high data rate of a single device eliminates parallel operation of multiple




8 16 MBIT MEMORY CARDS = 128 MBIT

FIGURE 3.9. BUBBLE MEMORY CHASSIS LAYOUT

| Data Rate (Mbps) | Duty Cycle | Memory CD Power Active | Inactive | Control CD & I/O Power | Secondary Power (W) | Primary Power (W) |
|---|---|---|---|---|---|---|
| Permalloy | | | | | | n = 65% |
| 1.4 | 100% | 51.01 | 0 | 20 W | 71.01 | 109.25 |
| 1.0 | 71.4% | 36.42 | 2.65 | 20 W | 59.07 | 90.88 |
| 0.5 | 35.7% | 18.21 | 5.95 | 20 W | 44.16 | 67.94 |
| 0.1 | 7.1% | 3.62 | 8.60 | 20 W | 32.22 | 49.57 |
| 0.05 | 3.6% | 1.84 | 8.93 | 20 W | 30.77 | 47.34 |
| 0.01 | 0.7% | 0.36 | 9.19 | 20 W | 29.55 | 45.46 |
| 0 | 0 | 0 | 9.26 | 20 W | 29.26 | 45.02 |
| Self-Structured | | | | | | n = 65% |
| 1.4 | 100% | 7.00 | 0 | 20 W | 27.00 | 41.54 |
| 1.0 | 71.4% | 5.00 | 1.43 | 20 W | 26.43 | 40.66 |
| 0.5 | 35.7% | 2.50 | 3.22 | 20 W | 25.72 | 39.57 |
| 0.1 | 7.1% | 0.50 | 4.65 | 20 W | 25.15 | 38.69 |
| 0.05 | 3.6% | 0.25 | 4.82 | 20 W | 25.07 | 38.57 |
| 0.01 | 0.7% | 0.05 | 4.96 | 20 W | 25.01 | 38.48 |
| 0 | 0 | 0 | 5.00 | 20 W | 25.00 | 38.46 |

TABLE 3.4

BUBBLE MEMORY MODULE POWER REQUIREMENTS

devices, and elimination of field coils reduces the device power.

### 3.2.3 Power Requirements

System power calculations are shown in Table 3.4. Permalloy power figures are based on existing 1 mbit devices and hardware, with 16 devices on a single card operating, Table 3.5. Controller and I/O power was assumed at 20 watts, higher than the EEPROM controller due to the added complexity of

| | Idle | Active |
|---|---|---|
| Sense Amp | 60 mW | 276 mW |
| Predrive | 169 mW | 642 mW |
| Driver | 0 | 620 mW |
| Op Drive | 350 mW | 350 mW |
| | 579 mW | 3188 mW |
| X 16 devices | 16 | 16 |
| | 9.26 W | 51.01 W |

TABLE 3.5

PERMALLOY BUBBLE POWER WITH EXISTING HARDWARE

controlling the bubble devices. Power supply efficiency was assumed as 65%. Each memory card is power gated, but one card is always powered when PSTROBE is active. This is necessary to meet the unknown incoming data rate with a minimum access time. Therefore, at low data rates idle power is dominant on the selected memory card.

Use of self-structured devices could significantly reduce power requirements due to its high speed, low power characteristics. Memory card power was based on existing permalloy support circuits, with a reduction due to the absence of large drive currents. The major factor in power consumption is not the memory cards but rather the controller, I/O and power supply.

### 3.2.4 Weight Estimates

A weight breakdown of a complete 1/2 ATR 128 mbit permalloy bubble memory chassis is shown in Table 3.6. Memory card weight was calculated with 16 bubble devices per card with LCC support chips packaging. The total weight of 44 lb. (20 Kg.) is also equivalent when 4 Mbit permalloy devices or 8 mbit self-structured devices are used in a like manner for capacities of 512 and 1024 mbits respectively. Use of high density bubble devices and elimination of the LCC packaging would reduce system weight to approximately 30 lbs. (13.6 kg), and reduce capacity by one-half.

## 4.0 TECHNOLOGY COMPARISONS

Of the possible memory technologies discussed, only the true nonvolatile technologies of EEPROM and bubble memory offer high reliability operation. Classifications within each technology were examined: NMOS and CMOS EEPROMs, and permalloy field access and self-structured bubbles. Maximum performance in terms of capacity, power and data rate is offered by self-structured bubbles. Implementation however, is not for some years to come. CMOS EEPROM can meet power, data rate and capacity goals in the near term with high density parts and packaging. Cost per bit is high, and hardness to radiation is low. Presently available permalloy bubble devices can meet capacity and data rate goals, but require large powers at high data rates. Radiation hardness is good, and the cost per bit is low. Each of these merits and pitfalls of each technology are examined further.

### 4.1 Capacity

Based on the system configurations discussed earlier, the projected system capacity versus time is shown in Figure 4.1 for bubble and EEPROM technologies. Introduction of higher density devices will provide the

| EQUIPMENT BREAKDOWN | ESTIMATED WEIGHT (LBS.) |
|---|---|
| BMM | 44.2 |
| Chassis | 10.19 |
| Front | .786 |
| Back | .874 |
| Sides | 1.940 |
| Cover Top | 1.174 |
| Cover Bottom | 1.532 |
| Hardware | .490 |
| Wedge Clamps | 1.454 |
| Motherboard | 1.21 |
| PC Board | .742 |
| Pins | .468 |
| I/O | .29 |
| Connectors | .229 |
| Wiring and Cables | .059 |
| PC Cards (10) | 28.76 |
| Heat Ladder | .133 |
| Connectors (2 100 pin) | .082 |
| PC Board | .407 |
| Components | |
| Control Cards | .309 |
| Bubble Cards* | 2.679 |
| Conformal Coat | .049 |
| Power Supply | 3.75 |

*.062#/bubble device

TABLE 3.6

BUBBLE MEMORY MODULE WEIGHT BREAKDOWN

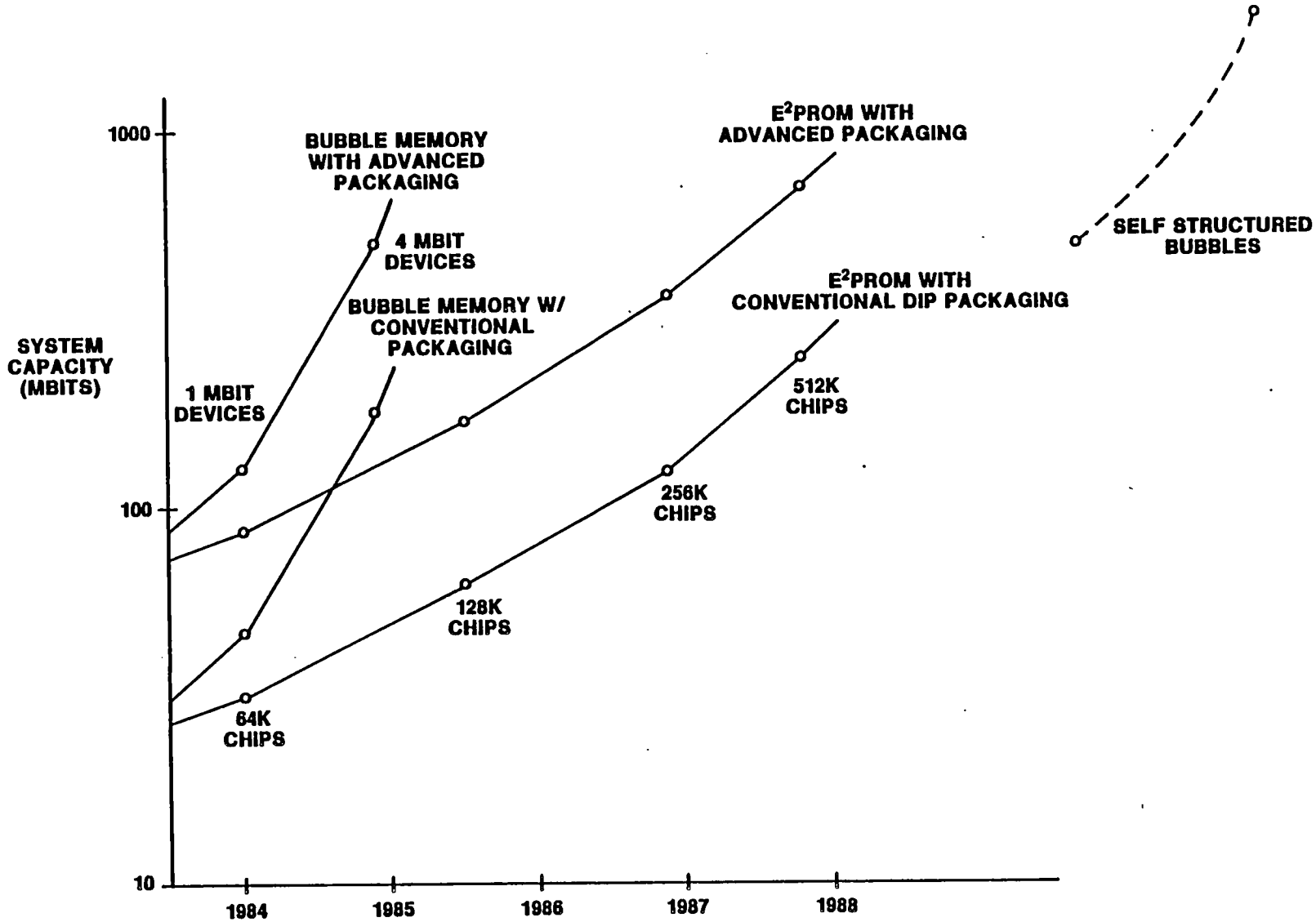



FIGURE 4.1. PROJECTED SYSTEM CAPACITY VS TECHNOLOGY

growth rate through 1990. Practical use of self-structured bubbles or other bubble types is not seen before this time. With 4 mbit permalloy bubble devices about to be released, a system capacity of 512 mbit could be realized in the near term.

## 4.2 Power Requirements

Previous power calculations are plotted in Figure 4.2. Very evident is the rapid power increase with data rate for permalloy bubbles and NMOS EEPROM, with both above 105 watts at 1.4 Mbps. This power level is almost completely independent of system capacity due to the power gating of unused memory cards. Low data rates or low duty cycle/high data rates would reduce power requirements to acceptable levels. The low power requirements of CMOS EEPROM is attractive, if cost and radiation goals can be met.

## 4.3 System Cost

Total system cost estimates were undertaken for systems build around permalloy bubble device and EEPROMs. Self-structured bubble devices are too early in the development stage to make a meaningful estimate. Estimates were made with present technology incorporated into a system as previously described which yielded 128 mbits and 92 mbits for bubbles and EEPROM respectively. By keeping capacity fixed and allowing insertion of higher density parts in the future, predictions on cost reductions were made. Estimates were made based on vendor quotes and trend predictions.

The relative cost of bubble and EEPROM systems is shown in Figure 4.3 The cost of the EEPROM system does not take into account the possible extreme measures necessary for radiation hardness of EEPROMs, and is therefore optimistic. A component cost breakdown for each system is presented in Table 4.1 with a bubble system as a reference.

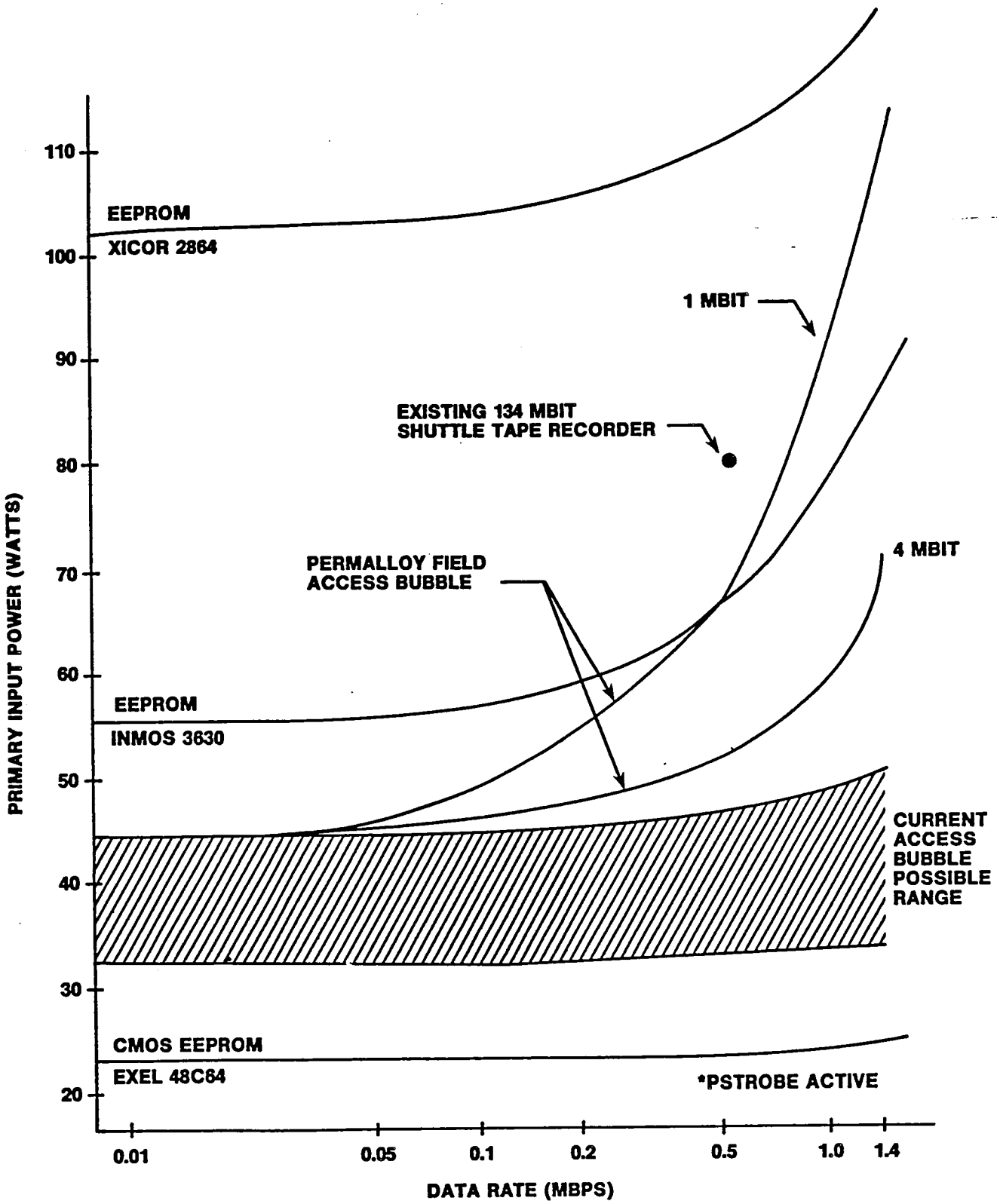



**FIGURE 4.2. MEMORY TECHNOLOGIES AND POWER CONSUMPTION**

(EEPROM Power is driven by write mode.)

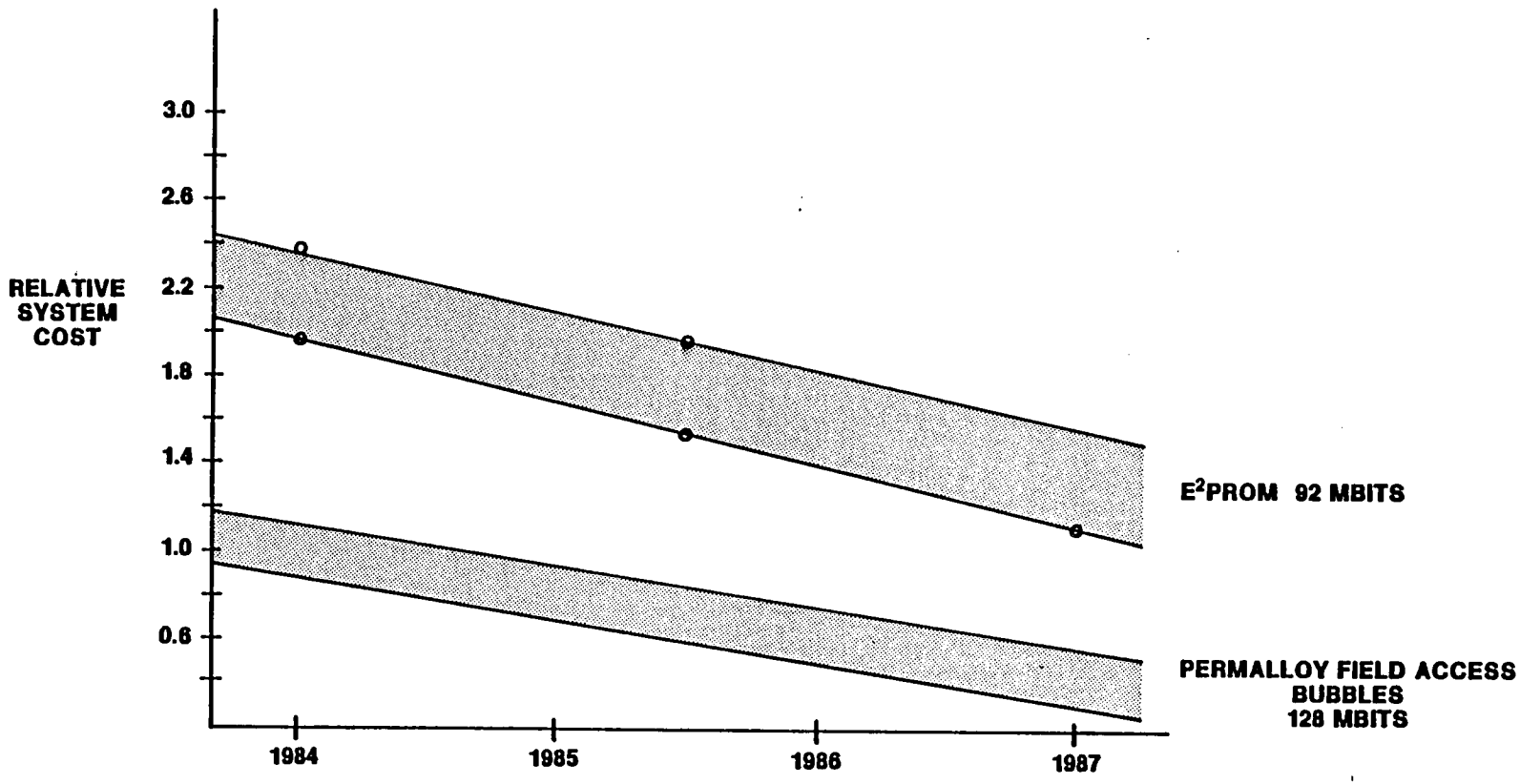



FIGURE 4.3. PROJECTED SYSTEM COST

| | 1 Mbit Devices (1984) | | 4 Mbit Devices (1987) | |
|---|---|---|---|---|
| Bubble Memory System | 1.000 | 100% | .459 | 100% |
| Chassis | .084 | 8.4% | .076 | 16.6% |
| Power Supply | .051 | 5.1% | .042 | 9.2% |
| PC Cards | .865 | 86.5% | .341 | 74.3% |
| Logic Cd. (2) | .025 | 2.5% | .021 | 4.6% |
| Bubble Cd. (8) | .102 | 10.2% | .040 | 8.7% |
| Bubbles & Support | .064 | 6.4% | .015 | 3.3% |
| PWB, Discretes | .038 | 3.8% | .025 | 5.4% |
| | 64K Bit Devices (1984) | | 512K Bit Devices (1987) | |
| EEPROM Memory System | 1.968 | 100% | 1.152 | 100% |
| Chassis | .084 | 4.3% | .076 | 6.6% |
| Power Supply | .051 | 2.6% | .042 | 3.6% |
| PC Cards | 1.833 | 93.1% | 1.034 | 89.8% |
| Logic Cd. (2) | .025 | 1.3% | .021 | 1.8% |
| Memory Cd. (7) | .255 | 13.0% | .142 | 12.3% |
| LCC EEPROM | .226 | 11.5% | .121 | 10.5% |
| PWB, Discretes | .028 | 1.4% | .020 | 1.7% |

TABLE 4.1

SYSTEM COST BREAKDOWN

The cost per bit of permalloy bubble memory is projected to decline by a factor greater than four by 1987[1]. This is due to advancement down the price curve and introduction of higher density parts. Since approximately 50% of the system cost is that of the bubble devices and support circuitry, a total system cost reduction of 50% could be seen by 1987. If a constant system capacity is maintained, higher density bubbles reduces the need for costly LCC on substrates packaging, further reducing the system cost to 46% of the present level.

The cost per bit of EEPROM is and will remain significantly higher than bubble memory. The cost of EEPROM's is expected to decline by a factor greater than six by 1987[1], leading to an 80% system cost reduction. However, this is still 150% above the cost of a comparable bubble memory system. As noted earlier, radiation hardening costs of EEPROM are not included here. Such costs could conceivably push component costs up five times, thereby increasing system cost 300%.

[1]Electronic Engineering Times, Feb. 13, 1984, P.54

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Note: References for Appendices B and C are included in their respective section.


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| 1. Report No. | 2. Government Accession No. | 3. Recipient's Catalog No. |
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| 172554 | | |

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| Feasibility of Self-Structured Current Accessed Bubble Devices in Spacecraft Recording Systems | April 1985 |
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| 7. Author(s) | 8. Performing Organization Report No. |
| G. L. Nelson, D. R. Krahn, et al. | |
| | 10. Work Unit No. |
| 9. Performing Organization Name and Address | 11. Contract or Grant No. |
| Sperry Corporation, Adv. Materials & Devices<br>P. O. Box 64525 CTC<br>St. Paul, MN 55164 | NAS1-16911 |
| | 13. Type of Report and Period Covered |
| 12. Sponsoring Agency Name and Address | Final 1982-1985 |
| National Aeronautics & Space Administration<br>Langley Research Center<br>Hampton, VA 23665 | 14. Sponsoring Agency Code |

15. Supplementary Notes

NASA Langley Technical Monitors: Dr. R. Stermer, Jr. and P. Hayes
Final Report

16. Abstract

This report describes a three year technical study of the self-structured, current aperture approach to magnetic bubble memory. Key results of this study include; 1)demonstration that self-structured bubbles (a lattice of strongly interacting bubbles) will slip by one another in a storage loop at spacings of 2.5 bubble diameters, 2)the ability of self-structured bubbles to move past intentional fabrication defects (missing apertures) in the propagation conductors (defect tolerance), and 3)moving bubbles at mobility limited speeds. Milled barriers in the epitaxial garnet are discussed for containment of the bubble lattice. Experimental work on input/output tracks, storage loops, gates, generators, and magneto-resistive detectors for a prototype device are discussed. Potential final device architectures are described with modeling of power consumption, data rates, and access times. Appendices compare the self-structured bubble memory from the device and system perspectives with other non-volatile memory technologies.

| 17. Key Words (Suggested by Author(s)) | 18. Distribution Statement |
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